



TECHNICAL REPORT 3016
June 2016

Nonvolatile and Cryogenic-compatible Quantum Memory Devices (QuMEM)

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ADMINISTRATIVE INFORMATION

The work described in this report was performed by the Advanced Concepts & Applied Research Branch (Code 71730), Space and Naval Warfare Systems Center Pacific (SSC Pacific), San Diego, CA.

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EXECUTIVE SUMMARY

This technical report presents the progress of the Space and Naval Warfare Systems Center Pacific (SSC Pacific) Nonvolatile and Cryogenic-Compatible Quantum Memory Devices (QuMEM) research project supported by the Navy's Science and Technology (S&T) In-house Laboratory Independent for Research (ILIR) Program. This report provides background information, motivation, technical progress, and technology transition efforts conducted throughout Fiscal Year (FY) 2014.

We describe the development of novel concepts for quantum memory devices to support quantum computation systems and advanced energy efficient digital systems. A key challenge is to design and implement novel devices that generate, protect, and store the quantum states involved in the computation process. Another challenge is to develop novel physical mechanisms to tune the quantum transport and potential Hamiltonian profiles to serve as a platform for the implementation of a desired quantum operation or algorithm.

The primary objective of the QuMEM project is to design and implement novel concepts, designs for solid-state, cryogenic-compatible quantum memory device chips where writing, reading, and erasing operations perform using fast (psec), low-voltage (mV) electrical pulses generated by on-chip computational devices. Here, quantum states are generated, tuned, and stored for computation. We increase the understanding of the memory storage process by characterizing the charging/discharging process, retention time, and endurance and how it correlates with design-driven theoretical calculations. Device chips designed for cryogenic operation with high-density memory arrays utilize emerging sub-10-nm fabrication methods, which are capable of on-chip integration with quantum computational devices. These devices are suitable for efficient tuning of the devices' Hamiltonian profiles by field-effect ion transport and tunneling processes, quantization effects, and exploiting superconductive properties. This research addresses key challenges of superconducting quantum computers with increased efficiency and scalability required to perform computation, which implement key information dominance functions. Devices are used in emerging architectures where novel device behavior and functionality are leveraged for unconventional signal processing, alternate neuromorphic architectures, and components for quantum communications protocols where quantum memory devices are critical.

Based on the effective electric field strength and ionic concentration/position, the quantum resonant transport and the Hamiltonian are tuned to achieve the desired superposition of quantum states. An advanced chip architecture incorporating the devices was developed with computational fabric based on qubits with built-in memory.

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1. INTRODUCTION

The development of a viable solid-state quantum memory device technology for quantum computation and communication has several challenges. These challenges reside at both the physical processes and the device construction. A key challenge we are addressing in this program is to design and implement novel devices that generate, protect, and store the quantum states involved in the computation process and develop novel mechanisms to tune the quantum transport and Hamiltonian to serve as a platform for the implementation of a desired quantum operation or algorithm. In addition, there are fundamental challenges to construction and processing of high-quality devices. QuMEM devices overcome these challenges, providing a viable technology to implement quantum memory in the solid state, accelerating the development of quantum systems for various information dominance strategies.

Quantum computation will significantly impact the U.S. Department of the Navy (DoN). Quantum computers would solve important and complex problems too inefficient and costly for classical computers to fix (Figure 1).. Quantum computers are expected to form a key element of the information dominance strategy. Conventional computing is reaching limitations in overall speed, energy efficiency, and functionality. Quantum computers can provide increased computational speed and energy efficiency by using parallelism and quantum algorithms.

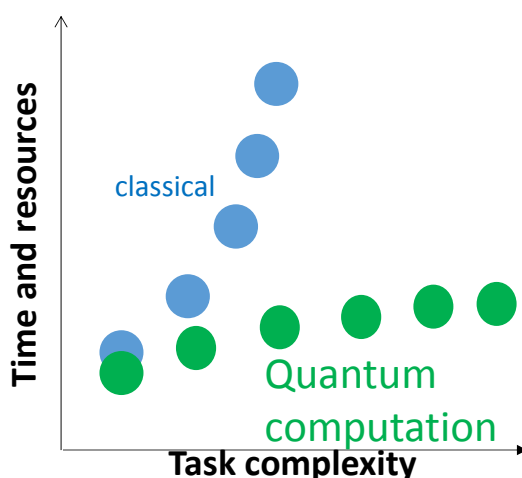


Figure 1. Quantum computation can solve complex tasks with the least amount of time and resources. Classical computing-based supercomputers require more resources to perform complex tasks in need of large amounts of energy, space, and cost.

A quantum bit, or qubit, is the building block of a quantum computer. Qubits are different from conventional bits; quantum behavior enables a superposition of states (i.e., $|0\rangle$ and $|1\rangle$) at the same time with varying occupancy probability. This property enables quantum computers to perform simultaneous operations on 2^N information states. The information process can use developed quantum algorithms that take full advantage of qubit properties. The end result is the ability to quickly solve hard problems with a limited amount of computational resources. For example, conventional computers do not perform efficient factorization, but quantum computers can factor large numbers, which is a critical function. The implications of efficient number crunching has relevance to key challenges of big data where conventional computers are reaching limitations in quickly solving key difficult problems, as shown in Figure 2.

Qubits vs. bits: Simultaneous operations on 2^N information states.

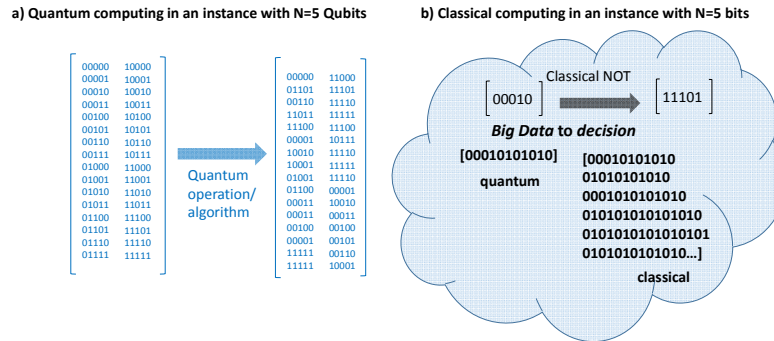


Figure 2. Computing with N qubits enables the simultaneous operation on 2^N information states where quantum operations and algorithms can be applied. Such capability could be useful to address big-data requirements where difficult information can be extracted fast.

The research executed by the QuMEM project addresses key technical challenges for the realization of quantum computers enabling cost-effective information dominance that can support many areas including the critical areas of cybersecurity/cyber situational awareness and information operations enabling the extraction and processing of useful information from big data accelerating the data-to-decisions process. For example, tightening the sensor to a warfighter cycle or finding important information among the big data, reducing access time from minutes to picoseconds and below. The impact of QC on the Navy's missions is profound and could solve certain important problems that classical computers can either not solve or are too inefficient and costly for practical use. Conventional computing based on classical devices is limited in speed and energy efficiency. Quantum computers provide significantly increased computational speed and efficiency while utilizing parallelism and quantum algorithms.

2. PROJECT OBJECTIVES

2.1 BIG/AGGREGATE-DATA SCENARIOS AND ROLE OF QUMEM DEVICES AND SYSTEMS

To show the growing need for computational storage solutions to address big-data challenges, we estimated the total data (bytes) collected by analog-to-digital converters (ADCs), a key component of a radio frequency (RF) receiver for two scenarios with varying sampling rate: data storage for a total time of 1 ms, and storage for a total time of 24 hrs. The total number of bytes shown in Figure 3 is expressed by the following expression:

$$Total\ (bytes) = (\#_{ADCs} * ADC_{bits} * F_{clock} * Time_{store}(s)) * \frac{8\ bits}{Byte}, \quad (1)$$

where $\#_{ADCs}$ is the total number of ADCs, F_{clock} is the ADC clock/sampling frequency, ADC_{bits} is the number of digital bits per ADC, and $Time_{store}$ is the total storage time.

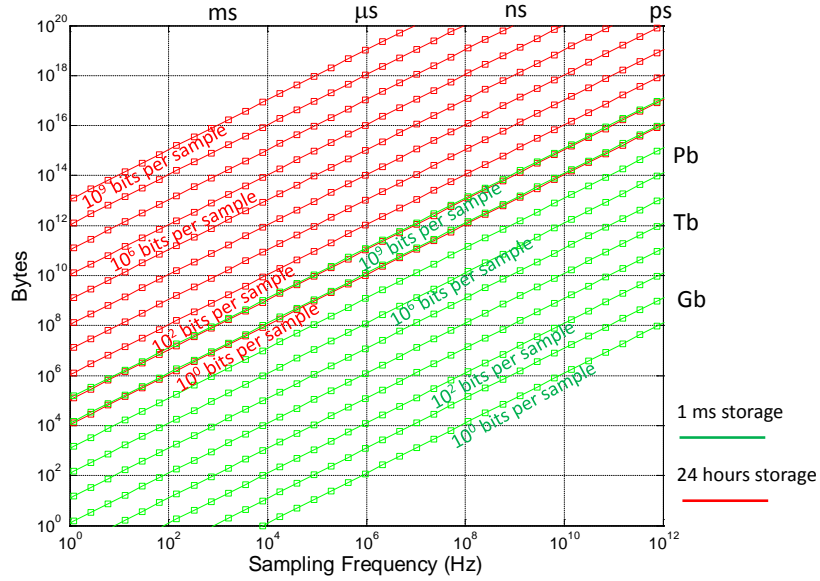


Figure 3. Total bytes generated for analog-to-digital converters (ADCs) as a function of sampling frequency. The collection and storage of all data each clock cycle (generated by a single gigahertz ADC) approaches petabyte scale each day.

A single ADC generating 10 digital bits/clock cycle at a frequency of 10 GHz generates 10 MB of data for each millisecond and ~ 1 PB of data for every 24 hrs. While storing data for 1 ms may be sufficient for certain applications, important information may be lost if all data is not stored (e.g., an agile radio frequency signal where key features are changing on the order of a single or few fast clock pulses). This analysis highlights the need for developing hardware technology for large-capacity storage and fast, efficient computational resources that can process (e.g., perform search) data in real time.

2.2 RECEIVER ARCHITECTURES WITH QUANTUM DEVICES

Figure 4 describes alternative architectures where quantum memory and computational technologies can play a key role (e.g., a receiver chain).

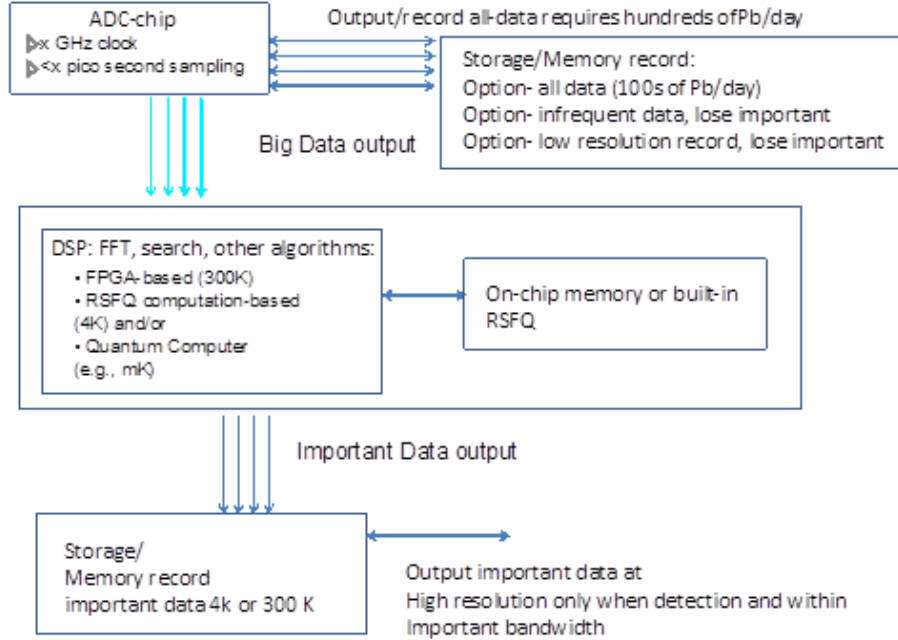


Figure 4. Leveraging memory devices at various stages in the receiver chain. A key function is the extraction of important information in real time.

For raw storage of generated data from a cryogenic-operated computer, memory storage technology could reside at room temperature, provided that interface electronics and loss in data transmission from cryogenic to room temperature maintains capability for storage at the intrinsic clock rate. High-speed memory will reside on a separate chip or on the identical chip as computational devices experience the same cryogenic environment, conditions for maximum performance.

If real-time computational capability or processing of the data is required, then a cryogenic-compatible memory storage technology is necessary, and must reside in the same environment. An on-chip memory device with computational technology would be beneficial for maximum speed and data transfer, especially where propagation loss may occur. When implementing key computational functions, including digital signal processing functions that leverage memory to extract key data, the key data extracted could then be stored at room temperature through memory storage technology. Figure 5 describes an overall information dominance system architecture where inputs are either RF or digital cyber data. In digital format, the data is storable and quantum computers are used for data mining during post-processing analysis or quasi-real-time modes.

Signal Processing/Cyber System Architecture incorporating QuMEM devices

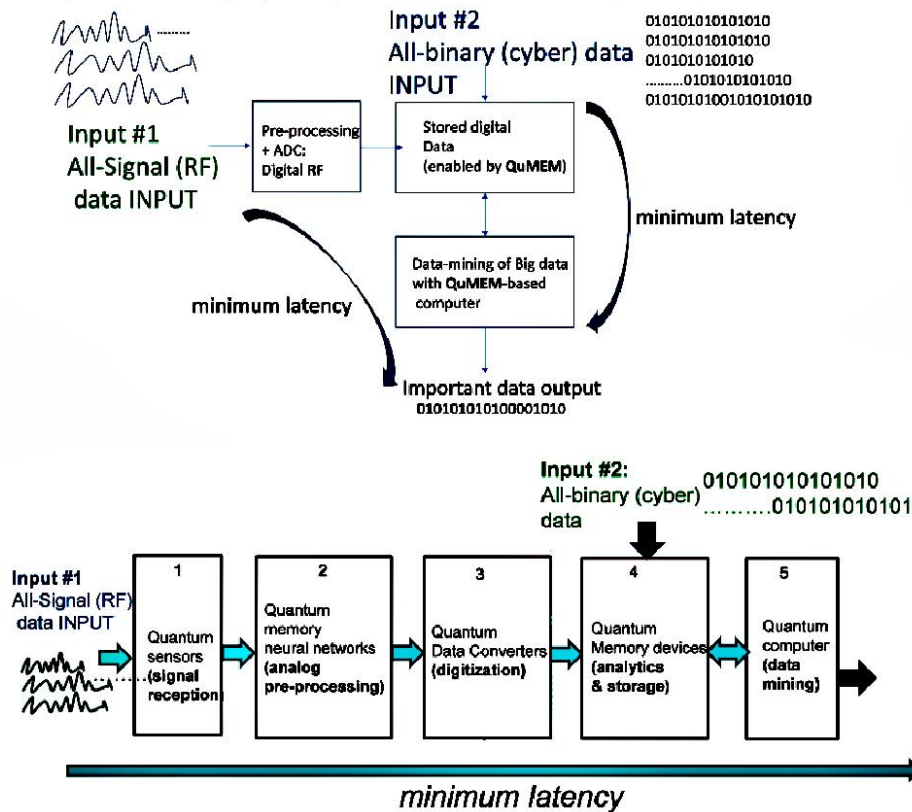


Figure 5. Signal processing/cyber system architecture with starting information inputs either RF-enabled or digital data. The architecture incorporates QuMEM devices in several stages.

Figure 6 compares measurements of the data collections and storage time for a commercial off-the-shelf (COTS) semiconductor-based, high-speed oscilloscope integrated with an external hard drive. The measurements show a lag between record bandwidth, storage time at the device-level, and interfaces. The integration of quantum devices with compatible devices can bridge this gap to ensure real-time processing.

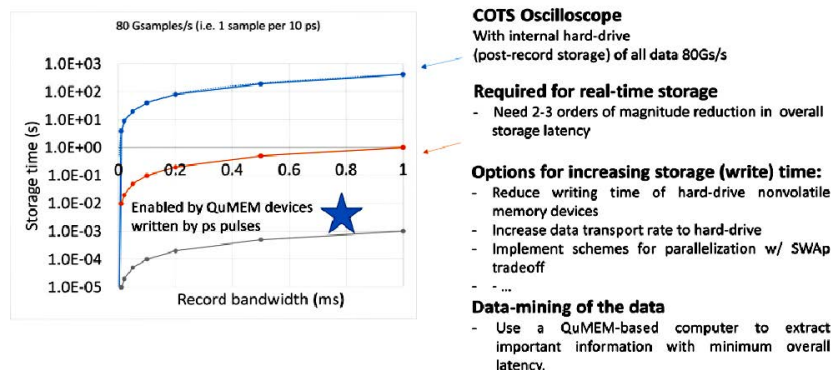


Figure 6. Measurements of the record/storage speeds for a COTS oscilloscope based on conventional technologies. Key factors limiting performance and addressable with quantum technologies are listed on the right panel.

2.3 NANODEVICE CHIP-BASED ARCHITECTURES FOR AUTONOMOUS LEARNING AND RECOGNITION

The QuMEM project team submitted a proposal to the Department of Defense's (DoD) Rapid Reaction Fund (RRF) program. The proposal recommends the development of a low space, weight, and power (SWaP) quantum, nanodevice-enabled chip with a hybrid network of emerging nanoscale devices, which perform autonomous learning and recognition of new signals and images. Each chip will implement a novel neural architecture with diverse memory devices integrated on-chip with low-power logic devices. The objective is to provide systems that perform fast, dynamic and autonomous learning, and recognition of new signals and images. The use of low-voltage, fast quantum-based memory, associated distributed quantum computing can increase architecture efficiency. The project addresses a key problem in the autonomous detection of new signals of interest among the massive amounts of data available to collect and perform these functions with low SWaP.

We are implementing a new neural chip architecture that is enabled by nanodevices and inserted near the sensor (see Figure 7). The architecture will utilize functional, diverse arrays of memory devices that store raw data and subsequently mark and learn key signals, images from the on-chip stored data. The project will leverage recent advances in high-density memory devices and energy-efficient logic.

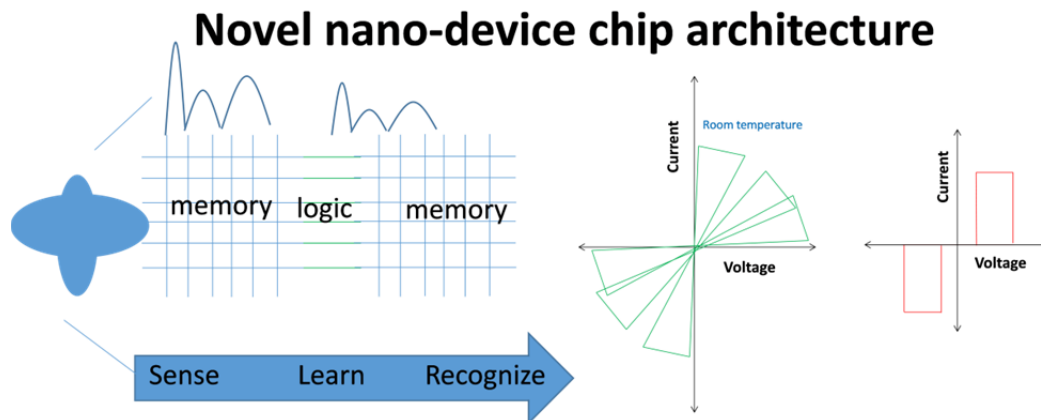


Figure 7. New nanodevice chip architecture for autonomous learning and recognition utilizing programmable memory elements.

The architecture accelerates the sensor-to-warfighter cycle by enabling a system to independently sense and recognize new signals and images in real time faster than the execution of a big data search following digitization (conventional approach). The architecture is used for deployment on small platform autonomous systems.

Key metrics include the efficient learning for detection, recognition of new signals and images, and the chip's SWaP. When comparing both hardware and software approaches, efficient learning and speed process are analyzed. We are making a demonstration that incorporates developed chip technology and that can create early signal image detection and recognition.

2.4 HIGH-PERFORMANCE COMPUTING (HPC)

As a result of the QuMEM project, we are producing the framework for a multiscale simulation of novel superconductor-based quantum devices that are nanoelectric and iconic. Through cooperation with private, commercial, and academia entities, we can advance modeling and simulation capabilities for quantum nanoelectronic and ionic devices. We can design technology from the

atomistic level to the device, circuit and system-level where superconductive and quantum processes are considered. Understanding quantum device performance and operation through fast, high-performance simulation will minimize the cost of an experiment. Figure 8 shows an example of this framework.

Advanced capabilities will enable rapid analysis of experimental devices, system improvement, and routes for improvement. Modeling and simulation development will improve quantum devices, and accelerate the development of information operation (IO), situational awareness, and cybersecurity-based systems within the DoD. This framework will require approximately 150 million core hours each year; this estimate is based on the number of cores (thousands) available on accessible machines, and higher performance core machines (millions), which we will leverage. The framework can integrate with industry Technology Computer-Aided Design (TCAD) software, open-source atomistic modeling (Density Functional Theory, Molecular Dynamics), quantum transport research software (NEGF), and Agilent circuit/systems modeling.

This framework addresses the challenge of developing novel approaches to high-performance computing and simulation based on nanoelectronic devices and circuits. Our multi-scale solution undertakes both temporal and spatial domains to accurately model coupled electronic-ion, electronic-phonon transport effects in designed superconductor-based quantum electronic devices, which start from the atomistic level to the device, circuit and system-level. Our approach develops a framework based on physics and implemented computational approaches, which focus on high-performance computing (HPC) systems—including hybrid multi-core and/or low-power central processing unit (CPU)/many-core graphics processing unit (GPU) architectures. The framework also evaluates the role of emerging quantum computing architectures.

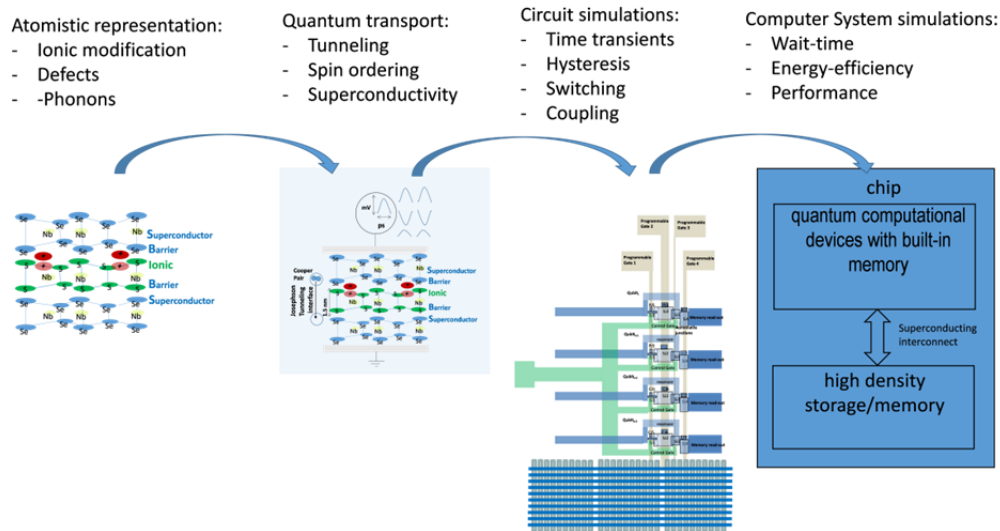


Figure 8. Multi-scale approach for high-performance computing integrating various levels from novel material to quantum device to circuit and the computational system. (Key computed metrics are highlighted.)

This collaborative project will deliver simulation framework to accelerate the development of nanoelectronic, computational architectures. The project will leverage experimental efforts already in progress, and provide test structures for the verification and validation (V&V) of atomistic models, and the calibration of analytical models. This project will make major contributions to publications, conference presentations, and patents. The project will also generate in-house expertise in the critical

field of quantum computation and create awareness of key challenges for commercial, private, and academia entities.

For example, there is a need to go beyond the conventional Ginzburg-Landau theory (formalism) for superconductivity to include coupled molecular dynamics (MD), Density Functional Theory (DFT), NEGF transport to accurately model electronic-ion, electronic-phonon transport effects, and analyze its support for quantum transport.

Recently, advances were made to incorporate molecular dynamic effects with quantum Langevin equation framework. While the proposed approach is promising, it can be improved to leverage the high-performance parallelism capability, which will implement a framework without requiring the simplifying features proposed. This will solve the problem to consider Hamiltonians from both electronic-ion, electronic-phonon contributions. We can also achieve the appropriate energy minimization under strong, weak field conditions simulated with real-time transport conditions. With accurate modeling at the atomistic level, we will advance the device simulation platform to link key parameters. This will influence device performance to include extraction of key parameters: transport velocity, diffusion coefficients, tunneling rates, scattering strength, and contributions from electron-ion/electron-phonon interaction to optimize a complex Hamiltonian with strong nonlinearity in its constituent components: $H_{total} = \sum H_{ph} + \sum H_{electron} + \sum H_{ion}$. These effects are important in the area of electronic materials where quantum devices we simulate will require a connection between the atomistic scale and the device-system-linking from picosecond scale transport, during cryogenic temperature, to system improvements derived from nanoscale devices. Also, leveraging the HPC capabilities available to include hybrid multi-core and/or low-power CPU/many-core GPU architectures, and the use of other accelerators with massive on-die parallelism. We will also evaluate how quantum computing can assist in the speedup of key elements in models.

We are advancing the parallelization methods (algorithm + multiprocessor hardware architecture) to address challenges amenable to computation in a distributed or tightly-coupled environment. HPC will play an essential role in the multi-scale simulations as the demand for memory, latency, and expected floating point operations per second require the available high-performance.

Due to the number of complex simulations needed (i.e., millions of atoms and millions of circuit elements), the maximum performance must exceed a personal computer. For example, memory requirements can quickly exceed hundreds of gigabytes once it surpasses a certain atom count or subsequent device count. It is also required that latency is kept to a minimum (e.g., shuttling data to and from memory regarding device attributes into the circuit and system simulations). Initially, we anticipated that available computational resources would be sufficient to develop POC modeling approaches and implement thousand-atom, thousand-device simulations, but there is a need for emerging HPC resources.

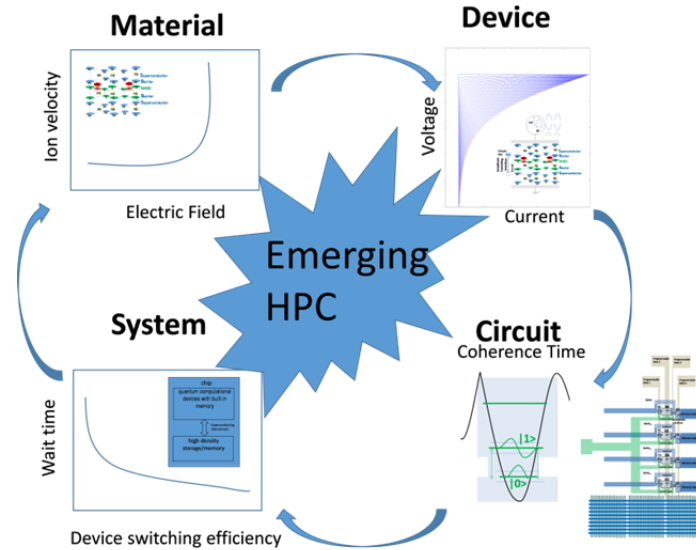


Figure 9. Example of a multi-scale simulation that demonstrates how small perturbation at the material, device-level translates to tangible reduced wait time of a systems vis-à-vis improvement in a device switching efficiency.

Table 1. Challenges for high-performance computing of quantum devices.

Challenge	Solutions needed and HPC roles
High electric field non-linear ion transport and defect generation/diffusion	Fast time-scale simulations of hetero-structures with many atoms requires demand on HPC resources (e.g., to perform molecular dynamics calculations to capture ionic transport while adjusting electrostatic potentials simultaneously to convergence).
Coupled molecular dynamics/quantum transport for device simulation	Coupled approaches require fast and efficient energy optimization to reach convergence requiring expensive HPC computational resource.
Circuit simulation linked directly to quantum transport solutions	Linking an advanced circuit simulation directly with the device output during real time requires high floating point operations per second and low latency computation resources.
System simulations linked to circuit simulations	Computing system level metrics, such as wait time and energy-efficiency with direct input from the circuit/device/material simulations, require full usage of HPC covering vast range of spatial and temporal scales, minimum latency, maximum memory, and greatest floating point operations per second.

3. COMPUTATIONAL ROADMAP

3.1 COMPLIMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS)

Conventional computers utilize transistor-based circuits operating at room temperature. These transistors are designed to utilize complimentary metal-oxide-semiconductor field-effect transistor (MOSFET) technology. The transistor count and performance increase enables the proliferation of CMOS-based microprocessors used in supercomputers, PCs, and various handheld gadgets. The operating principle of CMOS is thermal activation based carrier transport over a potential barrier to perform logic operations. To switch usefully between “on” and “off” states at room temperature (e.g., high- and low-drive current), a voltage >0.5 V is typically required for sufficient modulation. Due to several Moore’s Law limitations in performance, energy efficiency, and scalability, the operating frequency of a CMOS circuit is limited to approximately 10 to 20 GHz. While utilizing massive parallel arrangements of CMOS to perform, big-data processing is possible. This capability is at the expense of size, weight, power, and cost (SWaP-C), hence the proliferation of massive energy consuming data centers and supercomputer facilities. While the subthreshold switching of conventional CMOS can improve at cryogenic temperature, the thermal-based operation results in large variability and other nonideality that degrade, which is expected by conventional theory. Alternate designs are based on quantum mechanical tunneling. The mechanism of operation has the potential to reduce transistor operation to below 0.2 V, significantly decreasing power consumption as it scales V^2 .

3.2 RAPID-SINGLE-FLUX QUANTUM (RSFQ)

An alternative to CMOS technology is the rapid-single-flux quantum (RSFQ) logic digital technology. RSFQ is based on performing conventional Boolean logic and operations with ps, mV pulses generated via quantum effects in superconductor-based devices. Each pulse is generated from a superconducting loop containing a Josephson tunnel junction. Both maximum speed and minimum voltage are linked to the single-flux quantum parameter, a fundamental constant. A key advantage of RSFQ over CMOS is the ability to achieve fast clock rates (>100 GHz). A downside of the technology is the need to operate under superconducting conditions. At 4 K, the technology is reliable. There is the potential for an increase to 77 K and beyond to enable more widespread use. The technology is used to implement high-speed digital converters, and microprocessor building blocks (e.g., adders). The technology is also used for quantum computation control circuitry.

3.3 QUANTUM COMPUTATION WITH QUBITS

The alternative approach uses qubits where computations are implemented based on quantum algorithms. This approach does not have the potential for computational speedup in some cases. For example, conventional Boolean operations may provide significant speedup for problems specifically mapped to quantum memory leveraging unique quantum algorithms. Solid-state implementations are demonstrated using the Hamiltonian profile. The profile is generated by biasing Josephson junctions at unique voltages to create resilient 2-level systems for quantum information states $|0\rangle$ and $|1\rangle$. Table 2 summarizes the conventional and quantum computational paradigms.

Table 2. Challenges for high-performance computing of quantum devices.

Paradigm	Conventional (Transistor-based)	Quantum (Superconducting Josephson junction-based)	
Device/Architecture	CMOS (room T)	Rapid-single-flux quantum RFSQ (4 to 77K)	Qubits
Operation principle	Voltage > 0.5 V switches between high- and low-drive currents (10 to 20 GHz max).	Logic operations with ps, mV pulses (>100 GHz) generating via quantum process.	Potential profile at unique voltages generate resilient 2- level systems quantum information states. Parallelism and quantum algorithms.
Systems	Ubiquitous PCs/handhelds and servers	First-generation research and prototype computers (limited on/off chip memory). High-speed digital converters.	N/A
Key challenges	Performance, energy efficiency, scalability limit, and big-data processing (Brick Wall, End of Moore).	Novel memory devices, computing architectures and improved junctions, worldwide research efforts (more than Moore)	N/A

3.4 COMPUTATIONAL PERFORMANCE VS. ENERGY-EFFICIENCY SCENARIO

A key motivator for the utilization of qubits, and other quantum processes for computation, is the ability to reduce device counts and power consumption while concurrently improving the computation efficiency. The power consumed for computation, based on conventional devices, can be expressed as $2^N f V_{dd}^2$, where N is the device count, f the operating frequency, and V_{dd} the supply voltage. The strongest determinants are N , which is increasing exponentially, and V_{dd} , a usual constant with only slight reduction at ~ 1.0 V. The ability of quantum devices to process 2^N information states simultaneously enables overall power dissipation to be $N f V_{dd}^2$ where the role of qubits enables a reduced device count in addition to a typical operating voltage I in the millivolt and lower range. Figure 10 describes the power dissipation trends versus performance for both conventional and quantum computational approaches.

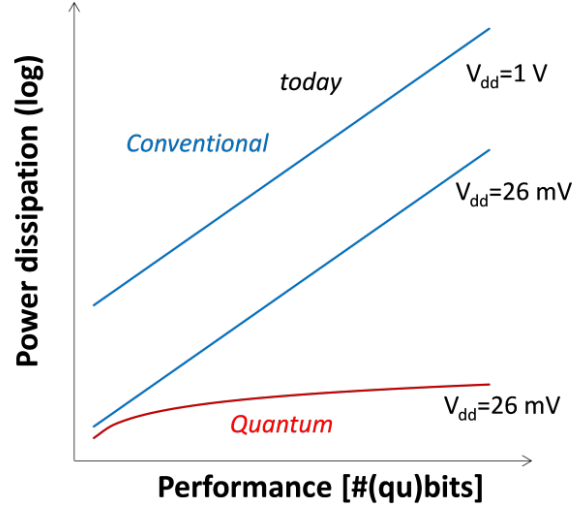


Figure 10. Power dissipation vs. performance for conventional and quantum computational technologies highlighting a key advantage in energy efficiency.

3.5 COMPUTER ARCHITECTURE

Another challenge to improve computational efficiency is to address the computational chip architecture shown in Figure 11.

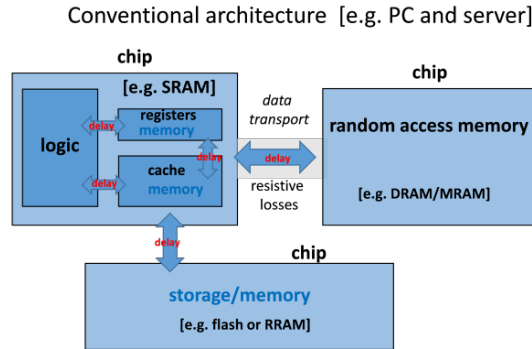


Figure 11. Conventional computing architecture highlighting challenges in utilization of multiple memory technologies located on separate chips, which increase latency.

The use of several types of memory located on separate chips is a concern. The need for different types of memory stems from the lack of a single-memory technology that has the speed, voltage and retention time required for required functions. Fast static random-access memory (SRAM) is usually located on a chip with computational devices, which has the role of both registers and cache. For conventional technologies, logic and memory devices are interconnected by resistive interconnect materials (metals) such as Cu, thus reducing the overall computational speed. There is also a need for additional types of memory such as dynamic random-access memory (DRAM); this is slower than SRAM, but is formed with a higher density and the use of storage memory such as flash memory, which is nonvolatile and retains its memory state. Due to material and voltage differences, DRAM and flash are commonly located on separate chips, thus increasing the resistive losses.

3.6 MEMORY DEVICE TECHNOLOGIES

To advance the overall performance and efficiency of quantum computation technologies, including RSFQ and quantum qubits, there is a need for novel devices and fabrication methods for memory storage devices. These devices should provide high-density, low-voltage, fast, and cryogenic compatibilities. Traditionally, memory devices are designed for room temperature operation, utilizing voltage levels required for charging, discharging from classical CMOS devices, >1 V. There is a challenge when designing and researching new memory devices to meet the requirements of quantum computation. Designing memory devices, specifically for quantum computation, requires matching a new set of requirements in speed, voltage, and temperature operation. Achieving these requirements simultaneously in a single device is challenging. Various leveraged devices are proposed to include flash, magnetic random access memory (RAM), and resistive random access memory (RRAM). The main bottleneck is due to physical constraints of the various approaches as well as material selections. Issues associated with existing memory technologies for quantum computation are shown in Table 3.

Table 3. Survey of memory device technologies and quantum memory highlighting key performance parameters and challenges.

Device Technology	Speed Write/Read/Erase	Voltage	Temperature	Market/Utility	Challenges
Flash	$\mu s - ms$	5–7 V	High	Nonvolatile (USB/drives)	>3 V, speed
DRAM/SRAM	ns	1–1.5 V	High	Classical comp. (PCs)	Volatile
Resistive RAM	μs	0.5–2.0 V	High to low	Research and development (R&D)	Speed, voltage, sensitivity, endurance
MRAM	100 ps – ns	0.5–1.5 V	N/A	R&D	Magnetic scalability >25 – 30 nm, req. off-chip
Proposed quantum memory	* ps	* <100 mV	*Room–cryogenic	Cryo/RSFQ/Quantum computation, compute compatible, multifunctional	Interfacing with quantum logic devices; new device designs

*Required for direct interfacing with quantum-based logic device technologies. Quantum states generated, tuned, and stored for useful computation.

3.7 FLASH

Flash memory requires relatively elevated voltages (>3 V) and microsecond-millisecond pulses to achieve the memory effect.

3.8 DRAM/SRAM

DRAM and SRAM are both volatile, requiring continuous voltage to refresh the state. Each device is limited in scalability and cryogenic compatibility due to the material system it utilizes.

3.9 MRAM

There are limitations on the overall scalability (>25 to 30 nm) and technology integration with magnetoresistive random access memory (MRAM); material integration requirements, large voltages, and current densities required for switching can create these limitations.

3.10 RRAM

While RRAM has the potential to achieve scalability, the typical resistive processes used for memory effects require large voltage and lacks sensitivity due to the use of conventional read processes.

3.11 QUANTUM MEMORY

There is a challenge to develop memory devices that can operate with significant improvement in speed and reduced operating voltage to directly interface with quantum logic devices. Also, devices should have the capability to achieve quantum confinement required for the generation and storage of well-protected quantum states. These requirements call for new quantum memory designs, based on device structures, which operate according to quantum processes during very low voltage; this may require integration of superconductors. There is a need for increased nonvolatility and coherence time to avoid constant refreshing of a conventional or quantum state. An increase in nonvolatility would enable long-term storage device use; this would also extend the overall time window for computation and analysis.

A unique opportunity exists to tailor the Hamiltonian to generate, store, and protect quantum states that are enabled with proper ion and host crystal selection under some conditions (harnessing the superconductor nature of electrodes). Ultimately, we would like a device that enables solid-state quantum memory, facilitates quantum computation and communication, and harnesses entanglement and superposition of states. However, we can use the technology in more relaxed conditions (i.e., voltage, temperature, material) as a cryogenic memory for superconducting digital computation and/or as the key element for energy-efficient information storage devices.

3.12 COMPUTATIONAL CHIP ARCHITECTURE QUANTUM MEMORY

The availability of a viable quantum memory device technology would enable future chip architectures (see Figure 12). On a single chip, both computational devices and high-density memory storage are all operating with mV/ps signals. As we describe later, there is a possibility to integrate into a quantum computational circuit with compatible built-in memory and high-speed digital logic or quantum information state processing. The interconnect is constructed from lossless superconducting material as the architecture is operated at a temperature where superconducting conditions are available; this results in a higher operating speed.

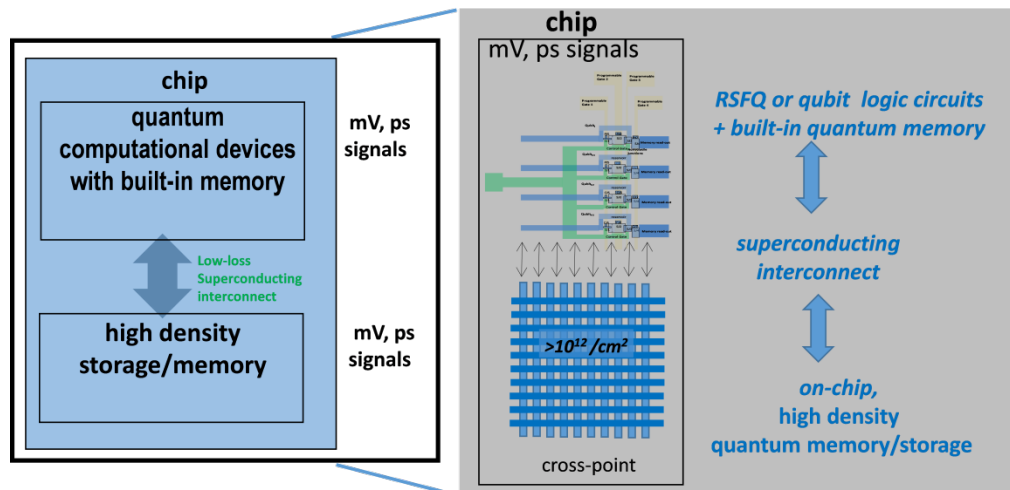


Figure 12. Chip computational architecture is incorporated on a single-chip qubit/RSFQ device in close proximity to memory and high-density, nonvolatile memory storage. Due to elimination of various lossy pathways, efficient qubit-based quantum computation or RSFQ superconductor digital logic can be performed.

4. DEVICE DESIGN AND SIMULATIONS

4.1 PRINCIPLE OF OPERATION: HOW DEVICE SHOULD WORK

Our patent-pending device concept exploits strong electric fields and quantum transport processes. The memory effect is based on an electric-field-induced (reversible) ionic separation/transport process in superconductor-barrier-ionic-barrier-superconductor (SBIBS) hetero-structure devices. The devices are optimized for the modification of the quantum transport and Hamiltonian profile where the ionic configuration is tuned by the applied electric field.

As described in Figure 13, the memory write process occurs through a voltage pulse, which generates a sufficient electric field to cause moderate transport of ions away from the superconductor/barrier interface. As a result, there is an appreciable modulation of the potential profile and quantum coherence length and current density across the device. The read process is through a low-voltage pulse sufficient to detect the critical current state, but below the threshold for achieving any additional ionic transport. The erase process occurs by applying a voltage pulse of the opposite polarity to transport the ions back to original configuration at the superconductor/barrier interface. This process returns the critical current back to pre-programmed conditions.

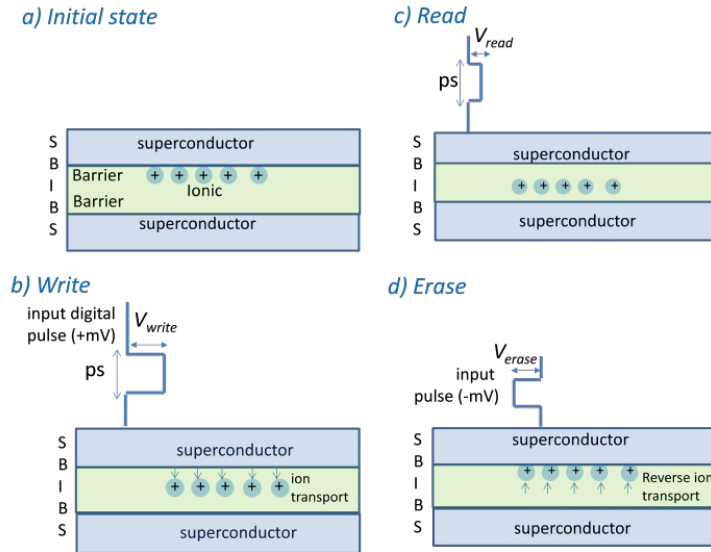


Figure 13. SBIBS device concept where the write, read, and erase memory functions are achieved through low-voltage pulses resulting in a reversible ionic transport of select ions away from the superconductor/barrier interface.

Due to the high sensitivity of the superconductor critical current on the detailed interface (ionic) composition and configuration (discussed in Sections 4.2 and 4.3), there is appreciable modulation of the overall superconductor critical current. In addition, the potential profile and effective Hamiltonian are tuned to provide for a platform to generate and store quantum information states for quantum computation and communication purposes. Variations of the structure are implemented to achieve the tunable profiles of a particular quantum algorithm (discussed in Section 4). In the non-superconducting state (e.g., room temperature), the device is used as a conventional high-performance, nonvolatile memory device. Here, the ionic transport process across the device generates conductance (resistance) modulation. This utility is also useful for implementing digital superconducting logic based on RSFQ pulses.

Where control of the (magnetic) spin state is necessary, both barrier material and ionic species are selected to produce the desired spin-ordering properties. Discovering proper structures to achieve the SBIBS device concept requires overcoming several challenges at both material and device level to include development of advanced thin films, techniques for ionic modification, construction of high-quality devices, and development of characterization protocols.

4.2 HIGH-FIELD IONIC TRANSPORT: ROOM TO CRYOGENIC TEMPERATURE

In the SBIBS device design, a key physical property is the electric field induced transport of ions across the barrier film; therefore, we closely examined these effects. We focused on the transport of ions across thin films for this research. Recently, the emergence of memory devices based on ionic effects has brought its study to the focal point. There is a balance between both applied electric field induced drift of ions, which largely determine the write/erase processes and an intrinsic diffusion or relaxation that largely determines the retention time of the memory state. A strong determinant of both of these processes is the potential barrier of the ions with respect to the host matrix. At high electric fields, non-linear ionic drift that significantly reduces the total write time. Due to a balance between optimal write and retention times, typically a nominally large potential barrier is engineered for room temperature operation with resistive materials and require an operational voltage >2 V.

In our design, we incorporate superconductor electrodes enabling quantum coherent transport to occur across the device through Josephson tunneling (Cooper pair and quasiparticle-based). We exploit the effect of low, cryogenic temperature on the nonlinear ion transport. Calculations demonstrate that at low temperature, a suitable potential barrier is selected to provide both fast write/erase times while maintaining a sufficient retention time due to the reduction in diffusive relaxation processes at cryogenic conditions (see Figure 14).

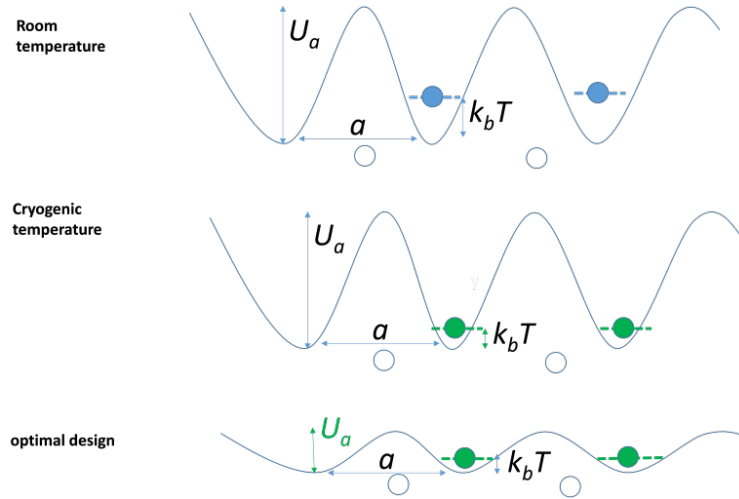


Figure 14. Schematic crystal lattice and point-ion for room temperature, cryogenic temperature, and an optimal design that favors both fast write speeds and long retention times under cryogenic conditions.

At low temperature, there is a requirement to operate at relatively large electric fields (> 0.1 MV/cm) to achieve the desired ion transport across the length of the device, which is attainable in ultra-thin films and hetero-structures at the designated low voltage.

The velocity of ions in thin films are described according to the point-ion models by the non-linear expression:

$$v \approx f a e^{-\frac{U_a}{k_b T}} \sinh\left(\frac{q E a}{2 k_b T}\right). \quad (2)$$

In the model, U_a is the activation energy for ion hopping, f is the frequency of hops, a is the periodicity of the arranged ions, and E is the electric field. In the expression for velocity, a key determinant for achieving a high ion-velocity is a high electric field and a small activation energy. While reduction in temperature results in a reduction in the ionic transport velocity, the effect is balanced by an enhanced velocity (Figure 15) and achieved through strong fields. The appropriate U_a is engineered.

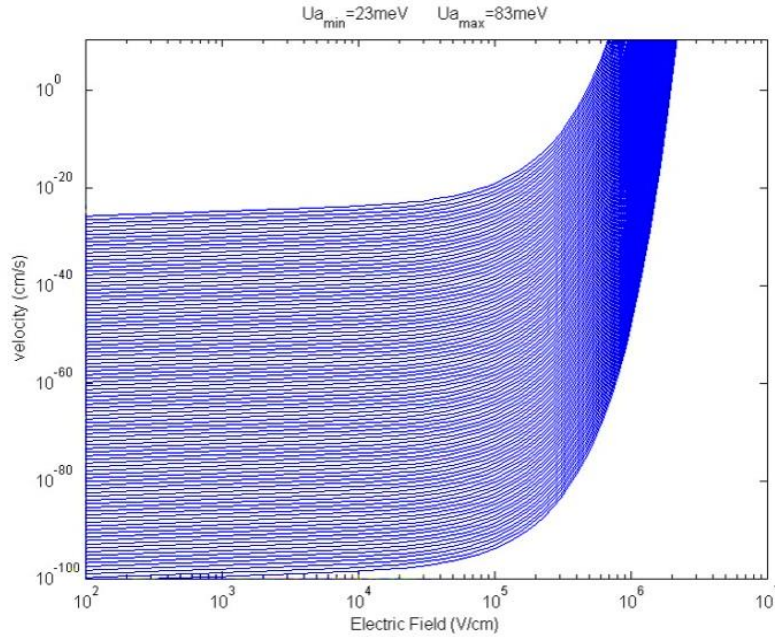


Figure 15. Simulated ion velocity vs. electric field for a range of barrier potential activation energy. There is enhanced nonlinear increase in ion-velocity for electric fields attainable in thin film devices.

4.3 MEMORY WRITE AND STORAGE TIMES

From the ion transport velocity, the switching speed or write time of the device can be expressed as

$$\tau_{write} \approx \frac{L}{v}, \quad (3)$$

where L is the required device (transport) length, and v is the ion velocity. Once programmed, the device will lose its state in

$$\tau_{store} \approx \frac{L^2}{D}, \quad (4)$$

where D is the diffusion constant for a loss of the stored state due to diffusion.

The ratio of volatility/switching speed ratio can be expressed based on the Ernst diffusion is

$$\frac{\tau_{store}}{\tau_{write}} \approx \frac{q}{k_b T} EL. \quad (5)$$

Figure 16 shows the calculated write time and Figure 17 shows the storage time vs. electric field for a range of activation energy spanning from 23 to 83 meV. Each calculation demonstrates fast (ps) write time and long >10-year storage. This is achievable with electric field levels that will not disrupt the ionic configuration.

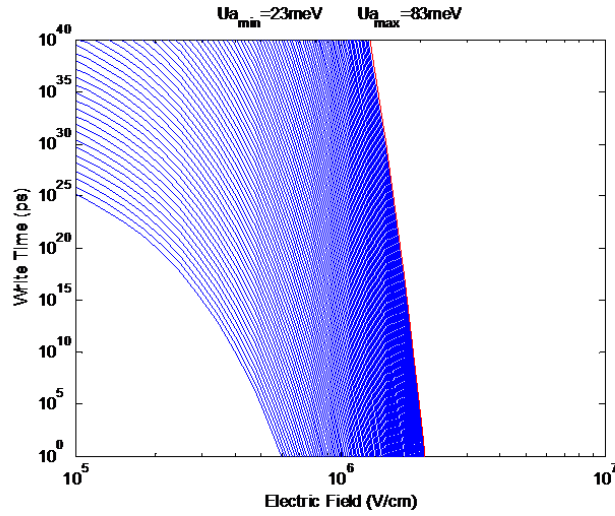


Figure 16. Calculated memory storage time of the ionic configuration vs. electric field for a range of ionic activation energies.

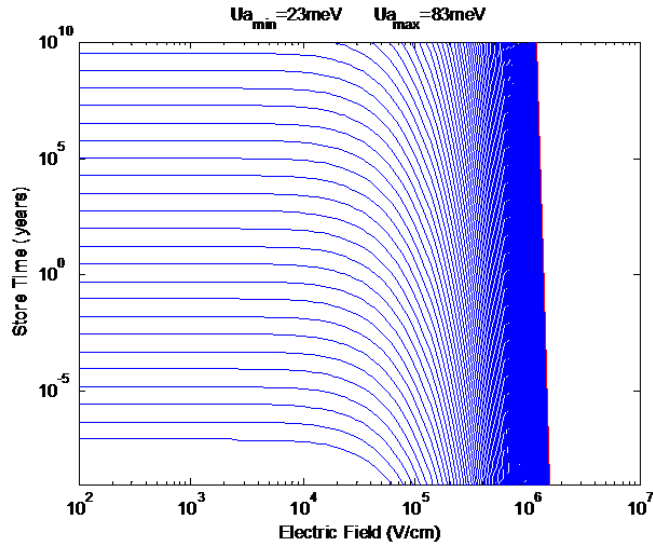


Figure 17. Calculated memory storage time of the ionic configuration vs. electric field for a range of ionic activation energies.

4.4 MODULATION OF THE JOSEPHSON COHERENCE LENGTH AND SUPERCONDUCTOR CRITICAL CURRENT WITH MODIFICATION OF BARRIER PROPERTIES AND IONIC CONFIGURATION

The critical current of a Josephson junction is a strong function of superconductor electrodes, barrier material, details of the superconductor/barrier interface, and the effect of embedded films or ions across the length of the device. Due to the quantum proximity effect, physics is affected by the constituent properties internal to the electrodes and the degree of transparency. The sensitivity of the critical current and energy profile is based on the device design. As a result, there is a physical mechanism to design superconductive memory devices. Electric and magnetic fields, provided by a voltage across the device, is an effective transduction method to result in modification of electronic, magnetic, and ionic configuration across the device.

A mechanism for controlling both critical current and Hamiltonian profile includes tuning the quantum transport coherence length, based on the ionic concentration, and positioning according to the superconductor/barrier interface. The expression for coherence length ξ_n for a normal metal barrier is

$$\xi_n = \left(\frac{D}{k_B T} \frac{\hbar}{2\pi} \right)^{1/2}, \quad (6)$$

where \hbar is the reduced Planck's constant, the diffusion constant $D = \left(\frac{1}{3}\right) v_F l_n$ with v_F the Fermi velocity, and l_n the mean free path in the normal material. Boltzmann constant is k_B and T is the temperature.

The critical current I_c is expressed as

$$I_c = \frac{4A}{\pi e \rho_n} \frac{|\Delta|^2}{k_B T_c \xi_n} e^{-\frac{L}{\xi_n}}, \quad (7)$$

where ρ_n is the resistivity of the barrier material, Δ the super gap voltage, and A is the cross-sectional area.

Figure 18 shows the mean free path vs. coherence length. Figure 19 shows the critical current vs. coherence length demonstrating orders of magnitude tuning with modest modulation of the coherence length enables by modulation of the mean free path. Each expression demonstrates the effect of altering a barrier material property on the superconductive property.

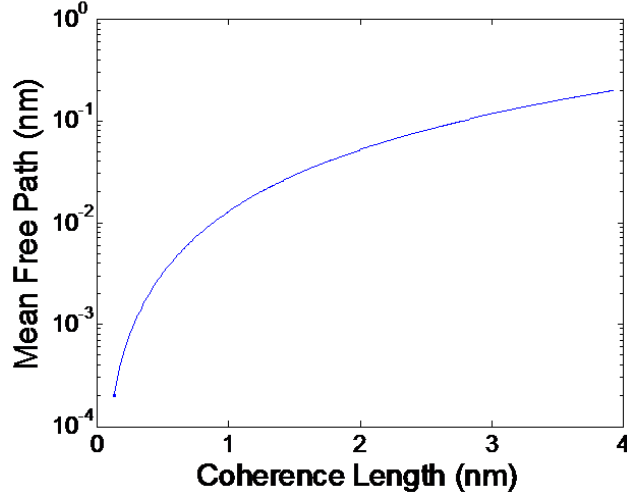


Figure 18. Mean free path vs. coherence length.

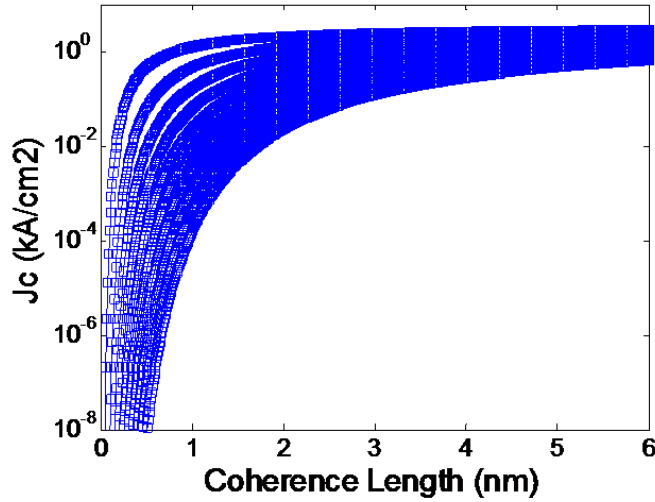


Figure 19. Critical current density J_c vs. quantum coherence length for a range of mean free path.

While Equations 6 and 7 consider the correlation between constituent materials properties and overall properties, generally, each equation results from coherence limit and critical current dependencies for metal-like barrier films. These films have an arbitrary charge density, which is a good approximation to the configuration with a sheet charge of ions. Here, ions at the effective Schottky barrier at the interface between the superconductor and the barrier. These expressions allow us to relate the density of ions to the critical current and coherence length by integrating the expression across the depth of the device length,

$$\xi_i = \int_{x=0}^{x=2a} \left(\frac{\hbar^3 \mu(x)}{6\pi e k_B T m^*(x)} \right)^{1/2} (3\pi^2 n_{ion}(a))^{1/3} dx, \quad (8)$$

where $\mu(x)$ is the position-dependent mobility, $m^*(x)$ is the effective mass and $n_{ion}(a)$ is the charged ion density, and $2a$ is the device length. Due to the ability to tune the position and density of ions

embedded in the barrier material, there is effective tuning of the effective coherence length, and consequently, a measurable quantity such as the critical current density,

$$I_c \propto \frac{1}{\xi_i} e^{-\frac{2a}{\xi_i}}. \quad (9)$$

In Section 4, we discuss the position-dependent potential energy profile across the device. In Figures 20, 21, and 22 we show the effect of ion density on the coherence length and critical current demonstrating capability for wide tenability.

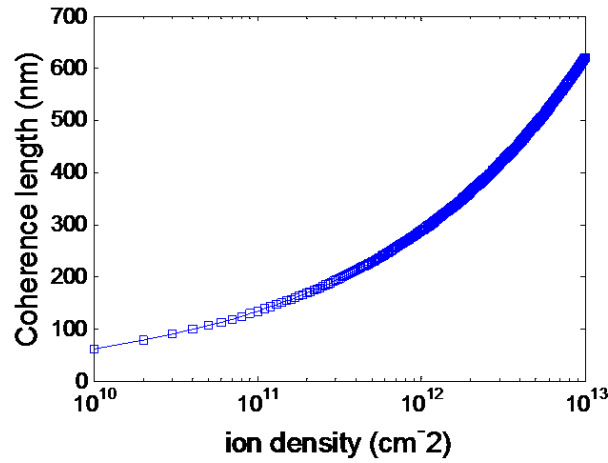


Figure 20. Coherence length vs. ion density.

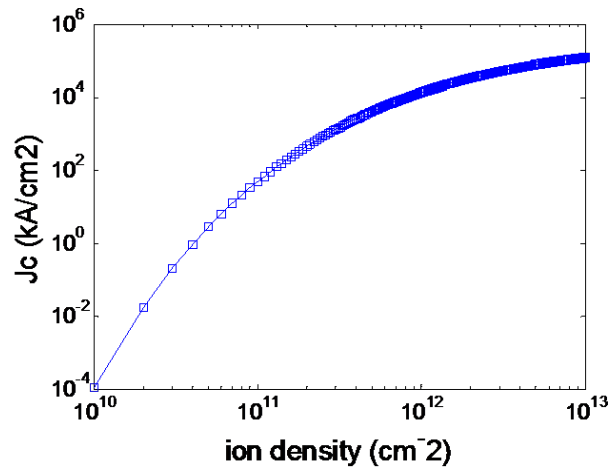


Figure 21. J_c vs. ion density.

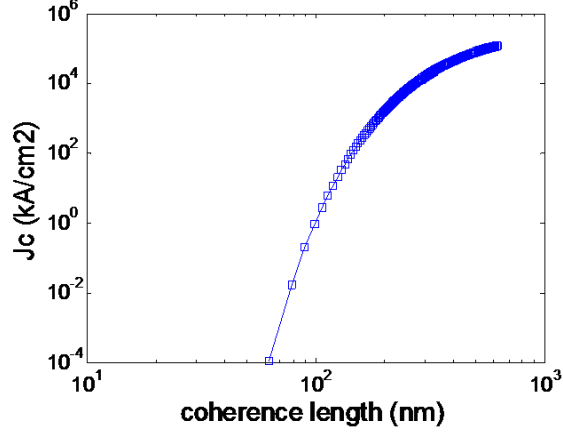


Figure 22. J_c vs. coherence length.

4.5 DEVICE CHARACTERISTIC MODELING

As discussed in Section 4.1, the superconducting quantum tunneling current across the SBIBS device is utilized to sense the memory state. This ability is useful as the Josephson effect in an adjacent logic device and is utilized to generate the fast and low-voltage pulses required to achieve the desired ionic transport. In addition, the electrostatic potential profile of the device generates the required potential for the generation of a 2-level quantum state system for performing quantum computations.

The impact of ions is a net modification of the ideality of the device; therefore, the effect of non-ideality, such as embedding ions, is related to the overall current voltage response. We developed an empirical model to describe the I-V characteristics with a free-fitting parameter that describes the overall ideality. The expression is calibrated to measurements in the literature of devices based on several materials. The model is used to describe the characteristics of an SBIBS device based on results described in Sections 4.3 and 4.4.

4.6 MODELING OF I-V CHARACTERISTICS

Recent advances have enabled the construction of Josephson junctions from a variety of superconductor electrodes, barrier materials, and fabrication approaches. The I-V characteristics of modern Josephson junctions usually consist of a superconducting current at 0 V and a voltage-dependent dissipation current for $V > 0$ with a connecting cross-over region or knee. While the superconducting current is due to the tunneling of Cooper pairs, the nonsuperconducting dissipative current is attributed to quasiparticle tunneling and additional thermal-assisted tunneling, noise, and trapping effects. The prevalence of such dissipation processes is strongly dependent on the material selection and fabrication process that results in varying junction ideality. While the cross-over occurs during a voltage range less than 1-mV range, and for some cases, $\ll kT$, its exact curvature can have a strong impact on the overall performance and reliability of a resultant circuit.

Various approaches were demonstrated to model I-V characteristics of Josephson junctions utilizing circuit elements, including RSJ, RSJN, and TJM models. While these models are often sufficient to approximate the dynamic operation of Josephson junctions, emphasis is typically not made to accurately describe the detailed cross-over region and dissipation current. Other developed models are often too computationally expensive for use in technology benchmarking analysis and circuit simulations and are not based on intuitive junction physical parameters. In this report, we present a physically-based compact model for the I-V characteristics of Josephson junctions that

utilizes an expression analogous to a Fermi-Dirac distribution function to connect continuously the superconducting to nonsuperconducting regions of operation. This includes the contribution of nonideality, which is a good approximation to the impact of ions embedded in the barrier material. From this representation, an extremely simple expression for the total current is derived that represents the characteristics of a quantum memory and only requires a few parameters inputted from measurements or derived from physical attributes. The model produces good agreement with the measured I-V characteristics of diverse Josephson junctions recently reported in the literature and is useful for examination of Junction ideality, technology benchmarking, parameter extraction, or circuit simulation.

We present a physically-based compact model for the current-voltage (I-V) characteristics of Josephson junctions applicable to quantum memory. We first analyze devices reported in the recent literature constructed with a variety of electrodes, barriers, and fabrication approaches. The model is based on a functional description analogous to a Fermi-Dirac distribution function and describes the characteristics continuously across the superconducting to nonsuperconducting subgap regime of operation including the nonideality observed as a nonabrupt cross-over and a voltage-dependent dissipation current. A few physical parameters are inputs, including critical current, subgap voltage, and temperature (inputted from standard measurements or derived from physical junction characteristics). A temperature-dependent fitting parameter is included and describes the Josephson junctions nonideality due to the contribution of additional thermal assisted processes and presence of ions; its extraction is useful for comparing the junction quality. Good agreement is obtained between the measured and modeled I-V characteristics of diverse Josephson junctions with varying degrees of intrinsic nonideality including, for example, Nb, NbN, MgB₂, and YBCO. We extend the model to describe the characteristics of devices with “extrinsic” nonideality useful for quantum memory devices.

In this modeling approach, the ratio of the voltage V drop across the junction to the subgap voltage V_{sub} is related to the difference in total current I and critical current I_c by a function analogous to a Fermi-Dirac type distribution function and is expressed as

$$\frac{V}{V_{sub}} = 1 - \frac{1}{1 + e^{(I - I_c)/\alpha kT}}, \quad (10)$$

where I is the total current, I_c is the critical current, V is the voltage across the junction, and V_{sub} is the sub-gap voltage. The expression continuously describes the superconducting and nonsuperconducting current including the cross-over region and the dissipation current for $V < V_{sub}$. The overall JJ ideality is included in the expression as a modification to the thermal activation term αkT , where α can be extracted by fitting the measured I-V data taken for a set of temperature conditions. Rearranging the expression and solving for I provides a simple expression for the I-V characteristics:

$$I = I_c + \alpha kT \ln \left(\frac{V}{V_{sub} - V} \right). \quad (11)$$

This use of a Fermi-Dirac type function to describe the relationship is physically based, as both Cooper pairs and quasiparticles are Fermions and obey Fermi-Dirac statistics. Alternative representation to describe noise effect, including Maxwell Boltzmann distributions and auto-correlation functions, may not accurately capture the contribution of quasiparticle tunneling. The alternative may only capture noise-related effects, where high-quality Josephson junctions are minor compared to thermal-assisted, quasiparticle tunneling contributions as the cross-over can occur over a voltage range $\ll kT$. Cross-over and subgap regions of Josephson junction I-V characteristics are

affected by various degrees of several processes, including quasiparticle tunneling, thermal-assisted tunneling, and noise. The combination determines the overall sharpness and the voltage dependence of the dissipation current. For example, Figure 23 shows simulations with varying values of α , V_{sub} at constant temperature, demonstrating various steepness in the cross-over and voltage dependence of the dissipation current.

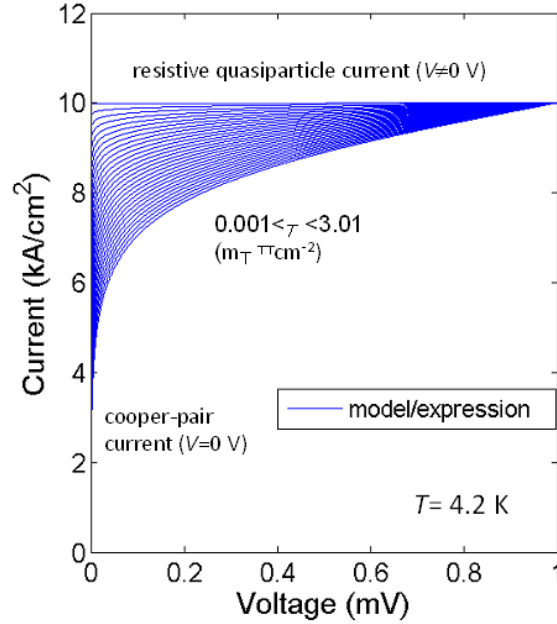


Figure 23. Normalized modeled current vs. voltage (I - V) characteristics with varying values of α spanning from 0.01 to 3.01 ($\text{m}\Omega^{-1} \cdot \text{cm}^{-2}$) in increments of 0.1 in the expression, $g = 2.0$ mV, $I_c = 10.0$ kA/cm², and $kT = 0.345$ mV/K.

We calibrate the model to Josephson junction data presented in the literature and constructed from Nb, NbN, MgB₂, and YBCO. Good agreement is obtained with appropriate selection of the model parameters as shown in Figure 24 for Nb, NbN, and MgB₂ with parameters from Table 4 and Figure 25 for YBCO with extracted parameters in Figure 26. While the introduction of novel electrode and tunneling barrier materials increases I_c , the junction ideality and/or superconducting energy gap reduces. YBCO-based, step-edge junction devices have the onset of Josephson junction behavior at ~ 77 K, and when cooled below 40 K, the associated nonideality is reduced. αI_c and V_{sub} continue to improve with further cooling towards 4 K. Vertical MgB₂ epitaxial sandwich junctions are operational at a slightly elevated temperature over Nb and have reported highly ideal characteristics at 20 K. NbN JJs have increased I_c over Nb; however, results show reduced V_{sub} . Introduction of improved barriers and dielectrics into traditional Nb devices can produce incremental increase in I_c without significant reduction in junction ideality. Figure 27 demonstrates applicability of the model for the case of a quantum memory device with tunable parameters and degree of ionic modification resulting in a hysteretic characteristic in forward and reverse sweeps.

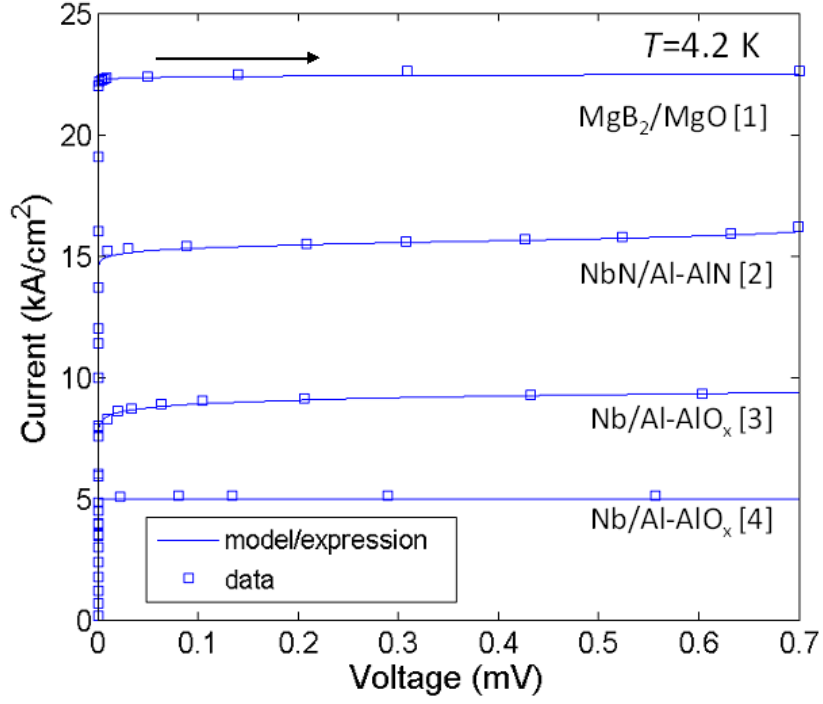


Figure 24. Normalized current vs. voltage using Equation 2 (lines) at 4.2 K for JJ devices based on MgB_2 , NbN, and Nb. For comparison extracted, forward sweep data is shown in squares with good agreement. Table 4 lists the input parameters used.

Table 4. Input parameters for I-V characteristics in Figure 24.

Device	α ($M\Omega^{-1}.CM^{-2}$)	V_G (MV)	I_c (kA/ CM^2)
MgB_2/MgO	0.12	2.02	22.51
$\text{NbN}/\text{Al-AlN}_x$	0.44	0.81	15.56
$\text{Nb}/\text{Al-AlO}_x$	0.34	3.23	9.63
$\text{Nb}/\text{Al-AlO}_x$	0.09	2.85	5.02

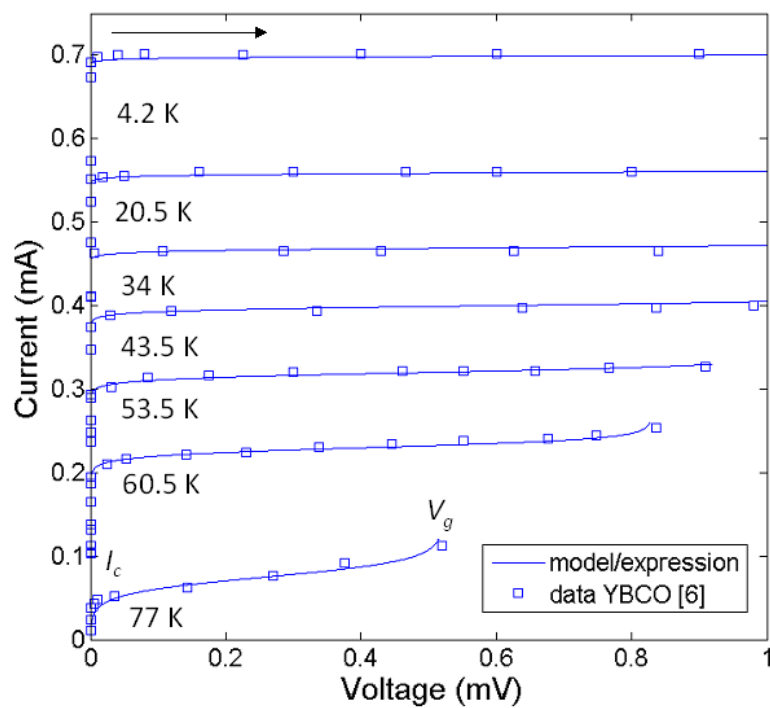


Figure 25. Modeled current vs. voltage (lines) and data (squares) in the 77- to 4.2-K range for a YBCO-based Josephson junction device. Good agreement is obtained between calibrated model/expression and data up to V_g .

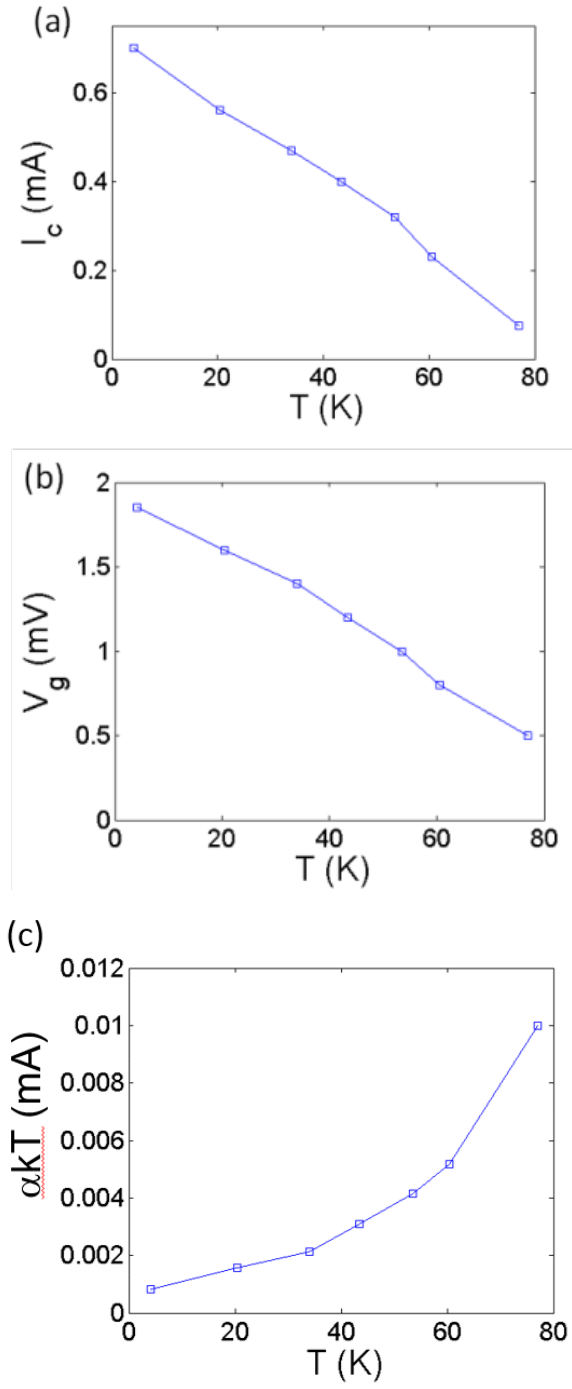


Figure 26. Extracted input parameters (a) I_c , (b) V_g , and (c) αkT based on fittings between model/expression and data (Figure 25) of a YBCO-based Josephson junction device.

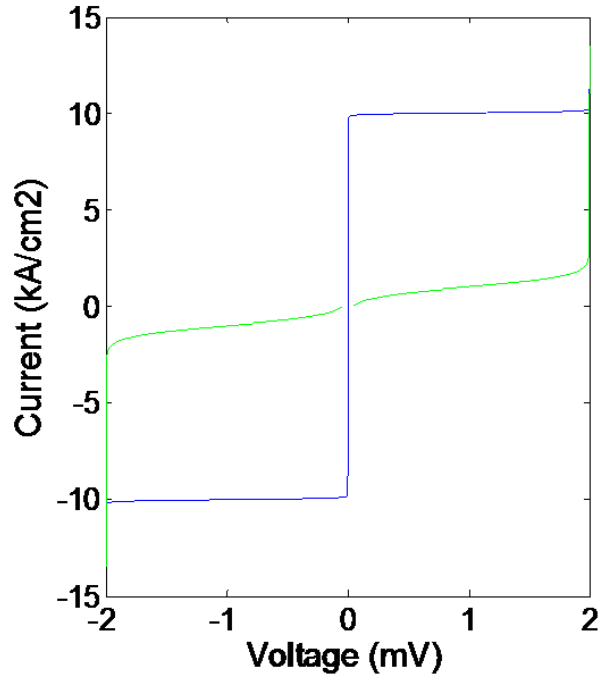


Figure 27. Modeled (hysteretic) forward and reverse characteristics representative of a quantum memory device.

In this section, we presented a physically-based model with a current-voltage for the I-V characteristics of Josephson junctions applicable across from the superconducting to non-superconducting subgap region of operation. The model is based on Fermi-Dirac statistics and results in a very simple and compact expression for the total junction current. We included an expression that captures the overall non-ideality and its fitting and extraction are useful for analyzing devices constructed from various materials and fabrication approaches. The project team utilized the model to analyze several devices in the literature and provide insight into the potential role of material innovations on future Josephson junction improvement.

5. QUANTUM COMPUTATIONAL CIRCUIT AND FABRIC DESIGN

5.1 COMPUTING CHIP FABRIC WITH NANOSCALE MEMORY

We developed a patent-pending concept/design for multi-junction reconfigurable, tunable quantum qubit circuits with computational functionality and built-in and internal memory/storage. The design utilizes quantization, charging effects, and gate-control introduced with the nanofabrication process to tailor the energy profile and electronic behavior enabling new multi-functionality. The design allows for new nonvolatile field-programmable configurations where quantum states are created and reconfigured through gate-control coupling, providing increased performance, complexity, resiliency, and reduced leakage. In addition to utilizing elements as the building block of future secure quantum computers, this invention enables the study of fundamental quantum information science algorithms not implementable with conventional structures by providing for many possible nonvolatile configurations and energy profiles. Our patent-pending SBIBS devices are the core of circuitry.

Quantum circuits formed from qubits are the building blocks of a class of quantum computers. A promising implementation is solid-state qubits. Due to physical limitations and intrinsic material properties, such qubits suffer from static behavior, state leakage and are prone to external effects that limit the reliability for large-scale computing architectures. While current current state-of-the-art designs were proposed for achieving programmable qubits using external influences and qubit-qubit couplings, they are limited in their ability to internally reconfigure with nonvolatile behavior. They have minimal ability for multifunctional operation internal to the junctions and/or qubits. Such designs rely on qubits built from a certain microscale junction technology to be interfaced to separate memory blocks built from an alternate memory device technology. These approaches can implement only specific types of computing that lack clean quantum behavior, such as the so called adiabatic with some level of programming capability. Moreover, these designs are functional in a limited window of operating conditions without a clear hardware capability for dynamic reconfiguration during the fabrication process and/or during operation. Alternatively, photonic implementations provide increased reliability in some cases, albeit lacking the capability for large-scale integration and robust routes for configurability. The disclosed invention provides novel concepts for advancing solid-state qubit implementations based on new approaches for achieving reconfigurable quantum circuits with built-in memory and improved reliability.

5.2 CONCEPT OF TUNABLE HAMILTONIANS

We advanced an alternate concept/design for a solid-state dynamically reconfigurable quantum computation/memory-chip fabric and underpinning quantum circuits, qubits, and superconducting junction device structures. An embodiment of the invention contains novel Josephson tunneling junctions produced utilizing high-fidelity He-ion beam nanolithography processes (see Figure 27). Junctions are sculpted on-chip with controllable nanoscale dimensions and with a precise in situ incorporated charge density providing the designer the capability to add junctions dedicated to both computational or memory functions in the same lithography process within the identical circuit. A typical junction consists of a high-temperature superconductor (HTS 1) film sculpted with an active Cooper-pair box region (HTS 1') with the dimensions of L_{active} and W_{active} in the sub-10-nm regime. In this size regime, quantization and charging effects modify the Cooper-pair box's electronic properties, resulting in significant energy-level splitting ($E_n \sim 1/d^2$). There is also an increase of the Cooper-pair Coulombic charging energy ($E_c \sim 2e^2/C$) to levels much greater than the thermal energy kT with expected well pronounced quantum oscillations. Junctions provide the necessary 2-level qubit system for performing quantum computation and the tunable re-configurability provides the ability to tailor-design the energy level properties for the desired functionality and speed while

setting the minimal leakage level. In addition, scaling of the Cooper-pair box introduces band-structure modifications that result in sensitive nanometer scale size tuning oscillations of the density of states, Josephson energy, a superconducting gap (critical determinants of the overall basic superconducting properties), current–voltage response of the junctions, and resiliency of the generated system level. The invention also enables the integration of our patent-pending SBIBS memory-device technology directly into the quantum circuits by introducing a controlled charge density through ionic modification in situ to the active region of the junctions during the device fabrication process. This enables the write/erase/read functions based on reversible ionic separation/transport process conducted through the appropriate pulses generated from on-chip devices.

The embodiment allows for on-chip quantum circuits to form and contain orders of magnitude of junctions with a desired active size and charging energy to produce a particular energy profile or functionality (e.g., for computation or memory). Figure 29 shows an embodiment of a quantum qubit-based circuit comprised of several (n) interconnected junctions (SJ_i, SJ_{i+1}, \dots) with gate controllable order parameters Δ_i and varying box size and charge density generating to first order a reconfigurable combined interaction energies E_J represented for all the junction pairs as $E_J = \int d^3r \sum_i^{n-1} \Delta_i^*(r) \Delta_{i+1}^*(r)$. The unique interaction energies are optimized for the optimal tunneling process (or Andreev reflections) and conducted with maximum efficiency, minimal external leakage, and other desired functions. This design includes additional junctions well-designed to facilitate the storing of an isolated or superposition of quantum states $|1\rangle/|0\rangle$ (e.g., utilizing nonvolatile memory SJ_4/SJ_5 junctions at the appropriate size scale and/or with the desired ionic modification for information state storage). The design includes a capacitive coupled control gate for simultaneously modulating the energy levels ($\Delta\delta$) of all junctions in addition to independent gates that allow the operator to dynamically reconfigure and create unlimited combinations of energy profiles as desired for facilitation and/or implementation of a particular state, quantum algorithm or encoding. Figures 29 and 30 show a multicircuit embodiment ($Qubit_i, Qubit_{i+1}, \dots$) of a building block fabric of a quantum computer chip. Figures 31, 32, and 33 show examples of expected configured energy profiles across several interconnected junctions achieved in the embodiment with a junction capable of read-out inserted with a deep well specifically for quantum information state memory/storage during the coherence time duration of the states. Figure 34 shows expected current–voltage characteristics across a multijunction with nonvolatile programming for a unique profile resulting in several resonances related to the individual junction tuning and its coupling strengths to adjacent junctions. The configured characteristics enable the designer to operate the quantum circuits in various regimes utilizing a combination and/or hybrid of charge, phase, and flux effects. In an embodiment, Figure 35 shows control-junctions (PJ_j, PJ_{j+1}, \dots) that are inserted in the process to function as the coupling junctions that interface between the active junctions (SJ_i) and gates. The use of the control-junctions isolates the active junction environment, thus minimizing leakage, error, and environmental effects, increasing the overall quantum coherence time allotted for performing the quantum computation/memory storage processes. The appropriate coupling and energy profile for resilient purposes are achieved by tuning the physical junction properties and electronic tuning. The vast flexibility in the design allows for achieving the standard set of universal quantum computation functions such as quantum-NOT/CNOT/SUM, as well as other functions needed for the particular purpose. The embodiment allows for the implementation of available algorithms, such as Shor's algorithm, in addition to others not yet available but inherently reconfigurable.

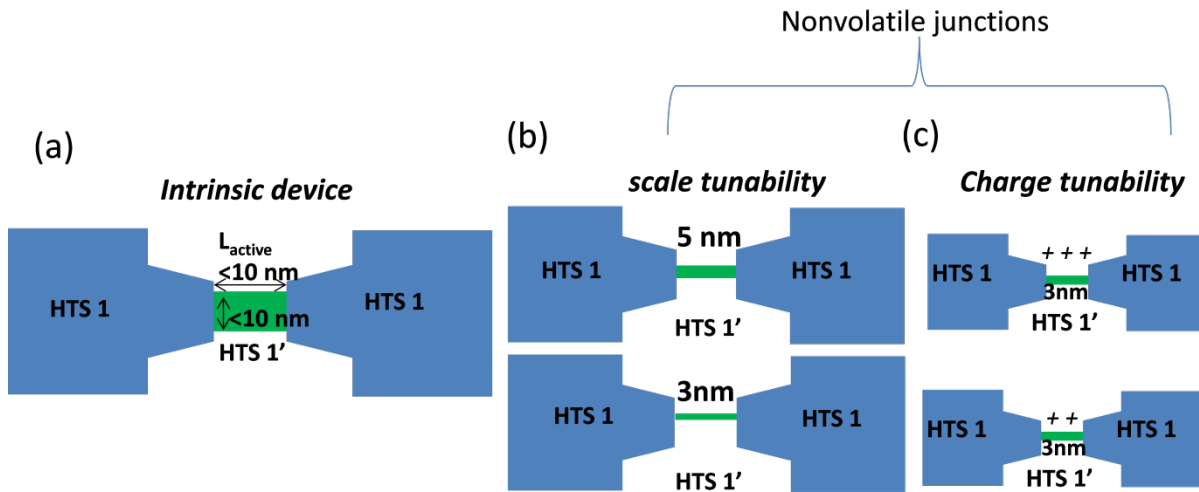


Figure 28. Schematic of deeply scaled devices with scale and charge tenability.

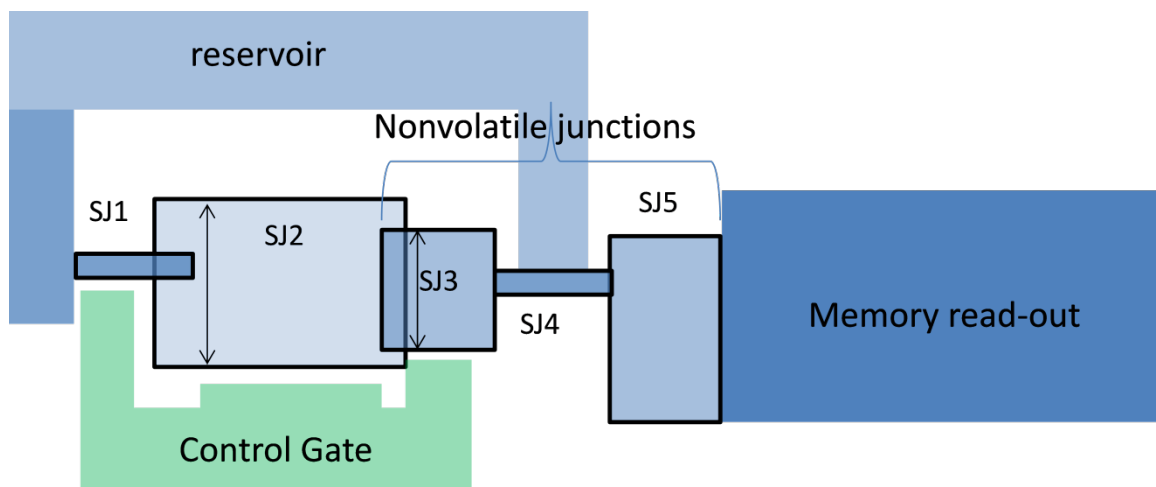


Figure 29. Qubit device incorporating QuMEM enabling built-in memory.

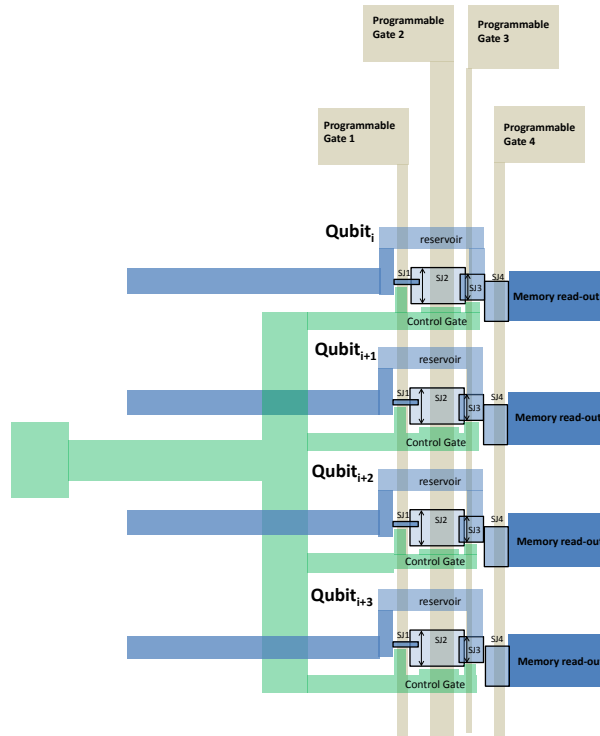


Figure 30. Chip fabric incorporating arrays of devices.

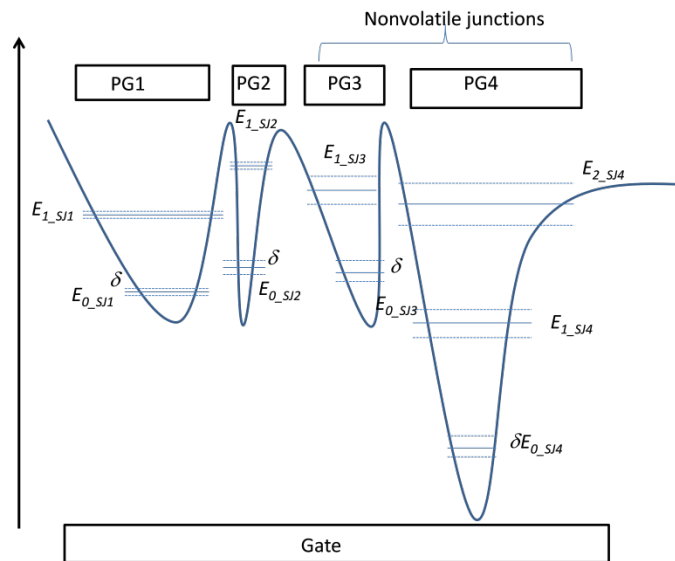


Figure 31. Tunable Hamiltonians across a device.

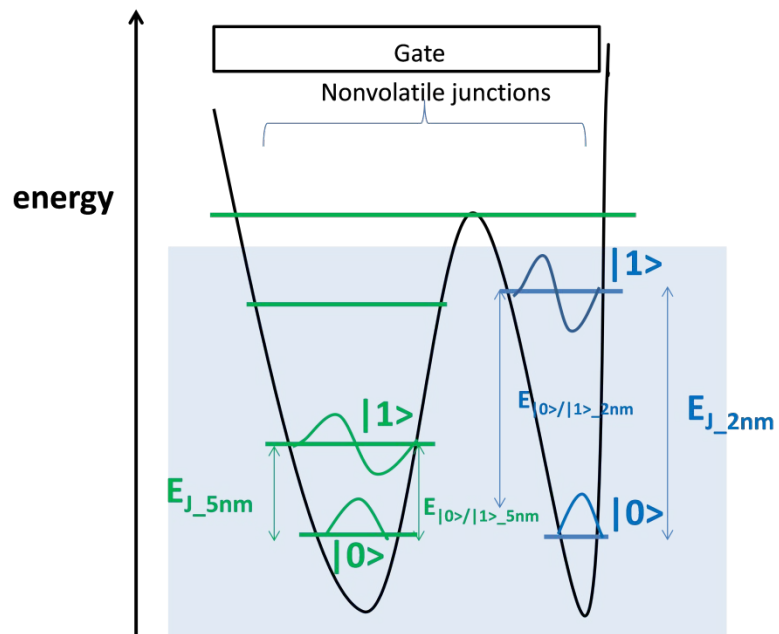


Figure 32. Leveraging quantization in the nonvolatile junctions.

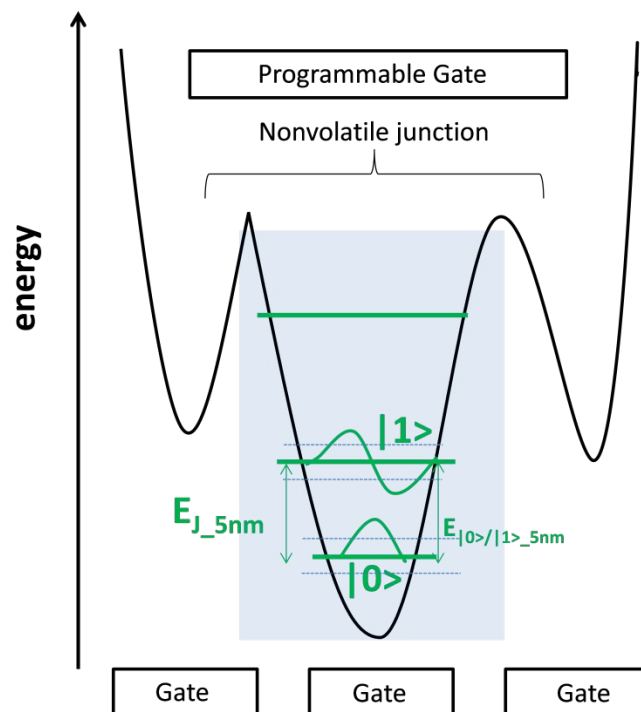


Figure 33. Programming the nonvolatile state.

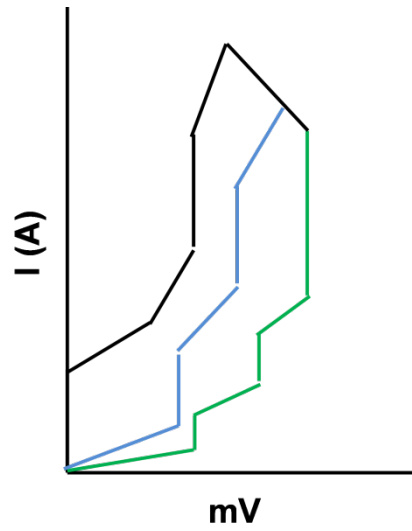


Figure 34. I-V characteristics upon tuning.

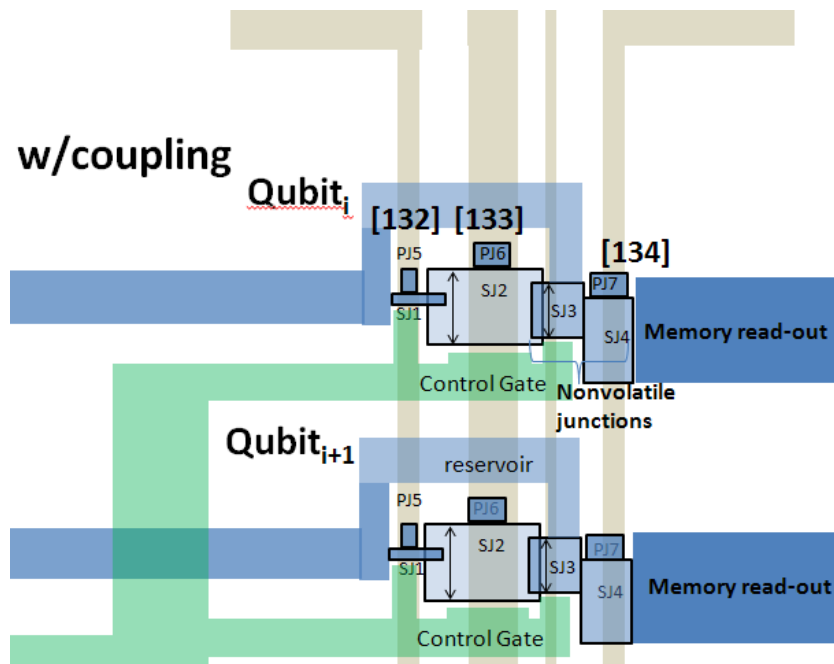


Figure 35. Close view of qubit integrating intercoupling.

6. QUMEM DEVICE CONSTRUCTION

Proof-of-concept (POC) devices were constructed to study our proposed device operation principles. We developed process flows for construction of devices constructed from a conventional low-temperature superconductor (LTS) based on aluminum and niobium material as well as HTS (YBCO) and emerging atomic crystals (e.g., NbSe₂). Our first process consisted of an Al/AlO_x/Al device formed with the barrier and ionic modification through plasma oxidation and exposure to CF₄. These devices were constructed at the San Diego State University (SDSU) Micro-electro-mechanical-systems (MEMS) laboratory with participation of the principal investigator in the MEMS Fabrication Course of the SSC Pacific Workforce Development Program supported by the Office of Naval Research (ONR) Naval Innovative Science and Engineering (NISE) Program.

6.1 MATERIALS AND CONTRACTS

In FY14, we acquired materials and executed contracts for device construction including:

- 4" SiO₂/Si substrates and wafer/sample holders
- Tweezers and wafer scribe
- Safety glasses, gloves, and fab wipes
- Probe tips
- Cleanroom tape
- Microscope calibration ruler
- YBCO substrates
- NbSe₂ crystal sample
- Participation in workforce development program at SDSU
- Contract for equipment utilization was awarded for processing at University of California, San Diego nano3 facility
- Mask set (four masks) from Photo Sciences, Inc.

6.2 MASK DESIGNS AND LAYOUT

A 4-level mask set was designed by SSC Pacific personnel and produced by Photo Sciences, Inc. The mask set enabled the complete construction of QuMEM devices, including electrode definition, dielectric isolation, and contact. Images of individual dies of the mask are shown in Figures 36, 37, 38, and 39. Complete tiled masks are shown in Figure 40 and photographs of delivered masks are shown in Figure 41.

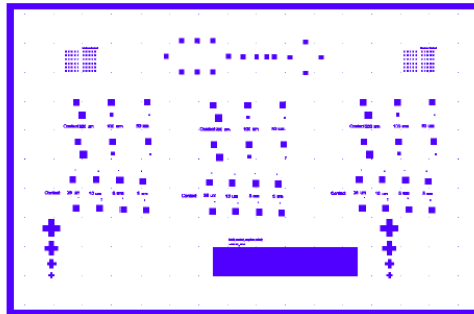


Figure 36. Top electrode mask design.

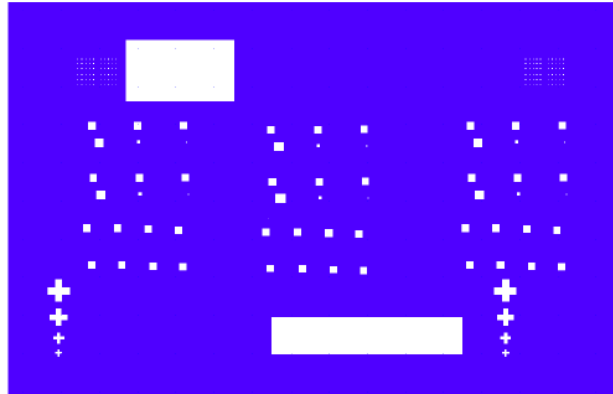


Figure 37. Contact mask (inverted).

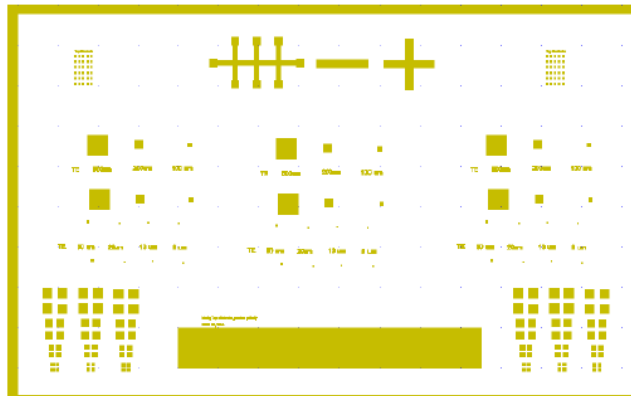


Figure 38. Contact mask.

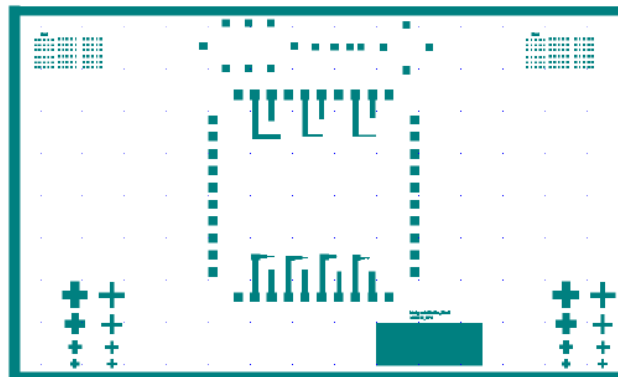


Figure 39. Metallization mask.

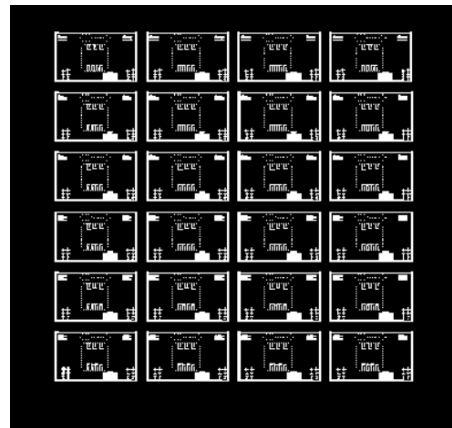
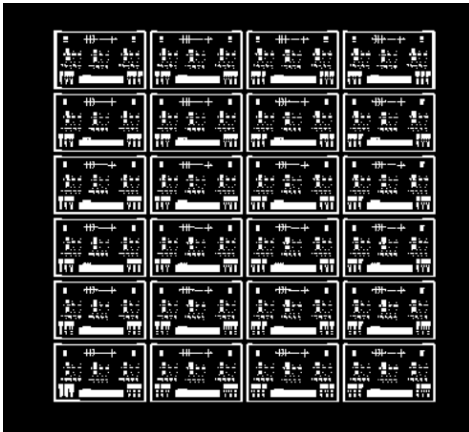
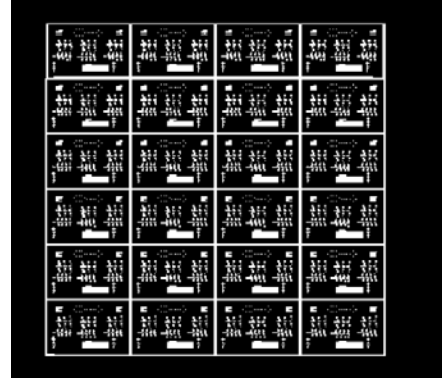
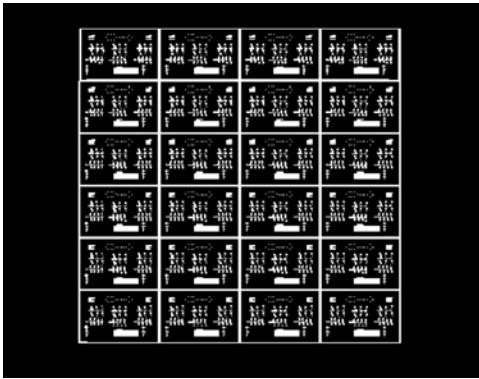


Figure 40. Masks with tiled dies patterned across the area.



Figure 41. Delivered masks as received from Photo Sciences, Inc.

6.3 PROCESS FLOW FOR AL/AL_{O_x}/AL DEVICES

In FY14, the PI participated in the workforce development program at SDSU. We developed a process flow for the construction of QuMEM device test structures by utilizing a combination of metal depositions, plasma exposures, photolithography, and wet chemical etching. Members of the MEMS laboratory performed device construction. Table 5 shows the process flow, equipment used, and how the flow included schematics of the processing steps.

Figure 42 shows a cross-sectional schematic of the constructed devices. Figure 43 shows a top-down scanning electron microscope (SEM) image of a completed device after photolithography and top-electrode definition through a phosphoric/acetic/nitric (PAN) etch clearing the aluminum down to the gold (Au) layer. Figure 44 shows a photograph of a complete device chip with four quadrants each representing a variation in the plasma treatment. Section 6 explains the electrical characterization of these devices.

Table 5. Al/AlO_x/Al device process flow.

Step #	Processing	Tool	Schematic							
1	Starting substrates from vendor, solvent clean (Acetone/IPA/H ₂ O)	Wet Bench at San Diego State University (SDSU) MEMS Lab	<table><tr><td>SiO₂ (Oxide)</td></tr><tr><td>P+ Si Handle Wafer</td></tr></table>	SiO ₂ (Oxide)	P+ Si Handle Wafer					
SiO ₂ (Oxide)										
P+ Si Handle Wafer										
2	Base electrode sputter deposition: (Ti/Au)	Sputter Deposition Tool at SDSU	<table><tr><td>Ti/Au BE</td></tr><tr><td>SiO₂ (Oxide)</td></tr><tr><td>P+ Si Handle Wafer</td></tr></table>	Ti/Au BE	SiO ₂ (Oxide)	P+ Si Handle Wafer				
Ti/Au BE										
SiO ₂ (Oxide)										
P+ Si Handle Wafer										
3	Base superconductor electrode evaporative deposition (Al)	Thermal Evaporation at SDSU MEMS Lab	<table><tr><td>Al</td></tr><tr><td>Ti/Au BE</td></tr><tr><td>SiO₂ (Oxide)</td></tr><tr><td>P+ Si Handle Wafer</td></tr></table>	Al	Ti/Au BE	SiO ₂ (Oxide)	P+ Si Handle Wafer			
Al										
Ti/Au BE										
SiO ₂ (Oxide)										
P+ Si Handle Wafer										
4	Plasma oxidation and treatment: O ₂ plasma + optional CF ₄	Plasma oxidation and treatment: O ₂ plasma + optional CF ₄	<table><tr><td>AlO_x</td></tr><tr><td>Al</td></tr><tr><td>Ti/Au BE</td></tr><tr><td>SiO₂ (Oxide)</td></tr><tr><td>P+ Si Handle Wafer</td></tr></table>	AlO _x	Al	Ti/Au BE	SiO ₂ (Oxide)	P+ Si Handle Wafer		
AlO _x										
Al										
Ti/Au BE										
SiO ₂ (Oxide)										
P+ Si Handle Wafer										
5	Top superconductor electrode evaporation	Thermal Evaporation at SDSU MEMS Lab	<table><tr><td>Al Top Electrode</td></tr><tr><td>Al</td></tr><tr><td>AlO_x</td></tr><tr><td>Al</td></tr><tr><td>Ti/Au BE</td></tr><tr><td>SiO₂ (Oxide)</td></tr><tr><td>P+ Si Handle Wafer</td></tr></table>	Al Top Electrode	Al	AlO _x	Al	Ti/Au BE	SiO ₂ (Oxide)	P+ Si Handle Wafer
Al Top Electrode										
Al										
AlO _x										
Al										
Ti/Au BE										
SiO ₂ (Oxide)										
P+ Si Handle Wafer										

Table 5. Al/AIOx/Al device process flow (continued).

Step #	Processing	Tool	Schematic
6	Mask 1 Lithography	Lithography Tool at SDSU MEMS Lab	<div><div>Al Top Electrode</div><div>Al</div><div>AlO_x</div><div>Al</div><div>Ti/Au BE</div><div>SiO₂ (Oxide)</div><div>P+ Si Handle Wafer</div></div>
7	Device definition wet etch (PAN etch)	Wet Bench at SDSU MEMS Lab	<div><div>Al Top Electrode</div><div>Al</div><div>AlO_x</div><div>Al</div><div>Ti/Au BE</div><div>SiO₂ (Oxide)</div><div>P+ Si Handle Wafer</div></div>

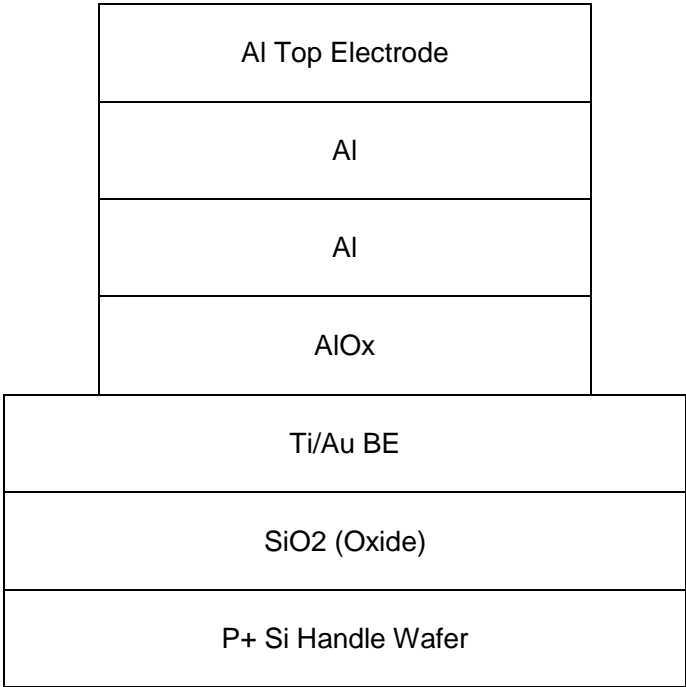


Figure 42. Cross-section schematic of constructed Al/AIO_x/Al devices.

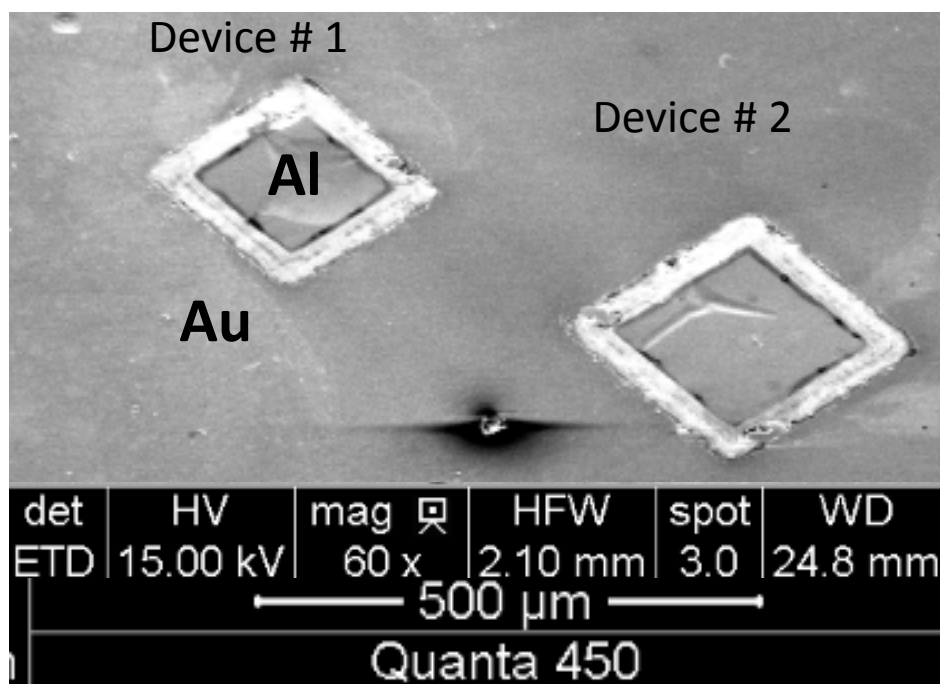


Figure 43. Top-down scanning electron microscope (SEM) image of a constructed Al/AIO_x/Al device as shown in the schematic in Figure 36.



Figure 44. Device chips formed with varying plasma oxidation conditions and exposure (e.g., O₂ and O₂+CF₄).

6.4 NIOBIUM-BASED DEVICES INCORPORATING ATOMIC LAYER DEPOSITION PROCESSES

We developed a novel patent-pending process for the construction of QuMEM devices heterogeneous with Josephson junctions. The process addresses several challenges, including achieving extreme device density scaling, device passivation/isolation, integration, and interconnection.

There is a need for new fabrication processes for high-density nonvolatile memory/storage devices that can operate with the performance and interface compatibility necessary for synergy with quantum computation processes. There is also a need for such devices to be integrated with on-chip Josephson junctions operating at cryogenic temperature. Recently, we disclosed a novel design for nonvolatile memory devices based on field-controlled ionic separation/transport in ultra-thin films embedded between superconductor electrodes. This disclosed invention provides an advanced process flow to construct such memory devices utilizing conventional semiconductor/superconductor device equipment available in nanofabrication facilities heavily leveraging emerging deposition techniques such as conformal atomic layer deposition. The process provides capability for the integration of ultra-thin films, development of the active tunneling region for memory devices, and/or Josephson junctions, and provides excellent protection of the active regions through subsequent processing steps and good isolation of the devices with minimal film consumption.

Current existing processes for construction of Josephson junctions typically utilize an anodic anodization process to achieve device passivation/isolation. Unfortunately, anodization results in consumption of ~60 to 80 nm of the superconductor film (e.g., Nb) and can cause degradation of the active tunneling barrier films and interfaces, limiting the minimum device area, final achievable circuit density, and overall circuit reliability. In addition, processes rely exclusively on the use of sputtered/evaporated films that require subsequent uncontrolled exposure to ambient to produce the tunneling barrier. Such formed barriers do not have the uniformity necessary to achieve ultra-low voltage and high-performance devices. These barriers create challenges for construction of the high-quality, ultra-thin functional film stacks required for various physical memory effects.

We developed a patent-pending process flow for the construction of a device unit is shown in Figure 45. Starting substrates are Si with a thermal oxide buffer layer and superconductor bottom-electrode thin film deposited by sputtering, pulsed-laser-deposition (PLD) or atomic layer deposition (ALD). An oxide isolation layer is deposited by low-pressure chemical vapor deposition (LPCVD) and active windows <10 nm are patterned by e-beam lithography and etched by wet or dry etching. The bottom tunnel oxide (3 to 5 monolayers of $\text{HfO}_2/\text{Al}_2\text{O}_3$), charge-trapping layer (1 to 2 monolayers of $\text{HfO}_x/\text{AlO}_x$), top cap (3 to 5 monolayers of $\text{HfO}_2/\text{Al}_2\text{O}_3$), and/or ferro-electric followed by an optional >20 monolayers of superconductor (e.g., NbSi) by atomic layer disposition (ALD) are formed in situ by alternating between thermal/plasma-enhanced/thermal ALD. ALD provides for conformal coverage in the well. Following ALD, a top superconductor electrode >50 nm is deposited by sputtering.

Following formation of the active device, region substrates are patterned and active devices were defined by dry-etching down to the oxide isolation layer protecting the active region from exposure to etch chemistry. Following substrate clean, a device passivation/isolation layer 5 to 15 nm is deposited through conformal ALD. Vias are defined and patterned and metal interconnect is deposited (resistive or superconductive) to connect high-density planar devices (Figure 46). A second oxide isolation layer 50 to 100 nm and bottom superconductor electrode can be deposited and the process repeated to form a three-dimensional (3-D) array of devices between top/bottom electrode of layers and top/bottom electrode of layerx+1 (see Figure 47). Conventional planarization is utilized to smooth the interlayer dielectrics between layers. In addition, the process produces conventional Josephson junctions with excellent isolation and passivation properties.

These junctions are integrated heterogeneously with memory devices in close proximity as shown in Figure 48 with their associated current/voltage characteristics for both computational and memory elements.

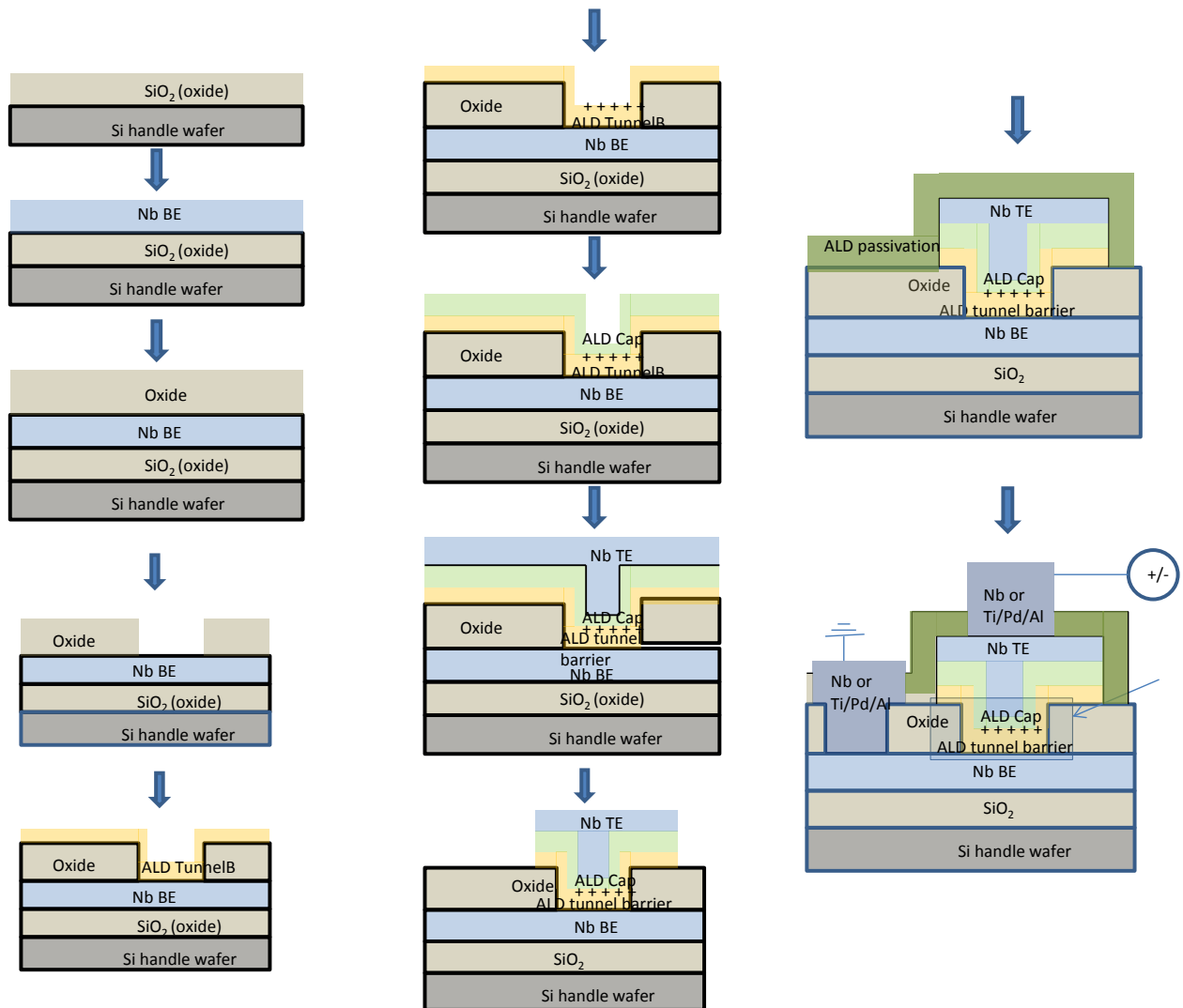


Figure 45. Process flow for Nb-based devices incorporating ALD for the deposition of the tunneling barriers and for passivation/isolation of devices.

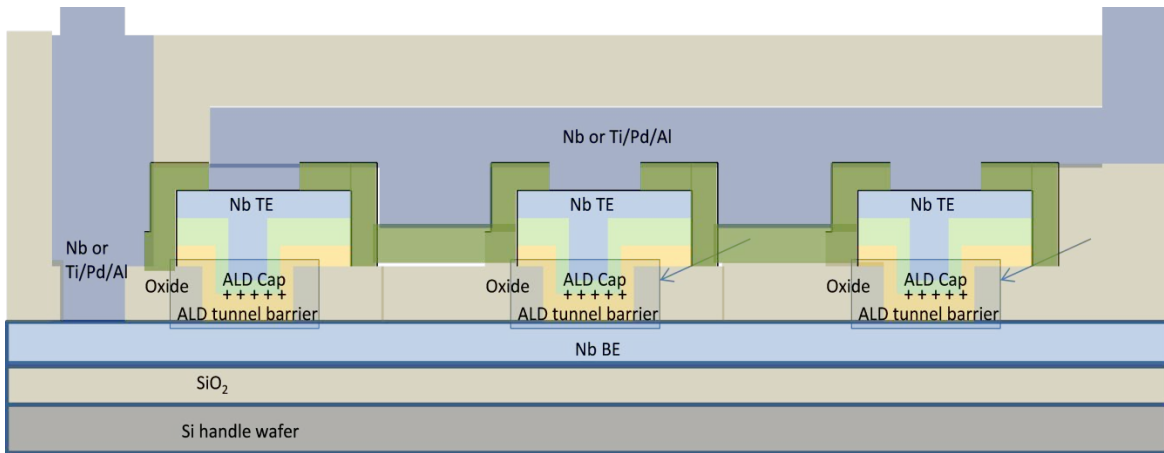


Figure 46. High-density integration of quantum memory devices with minimal device–device spacing.

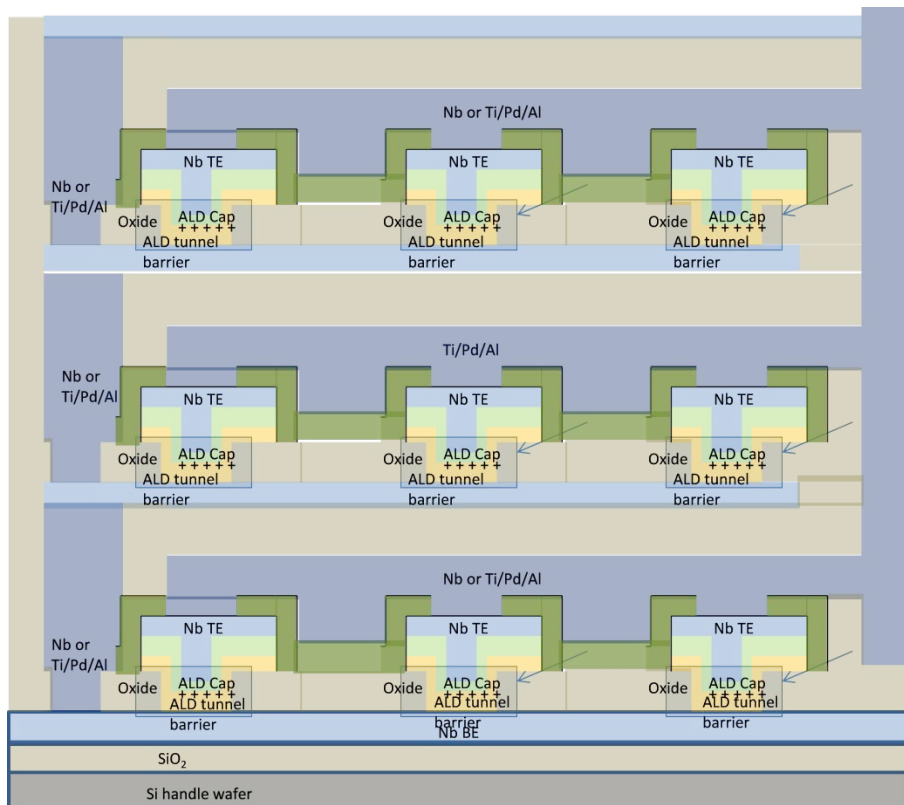


Figure 47. High-density 3-D integration of QuMEM devices.

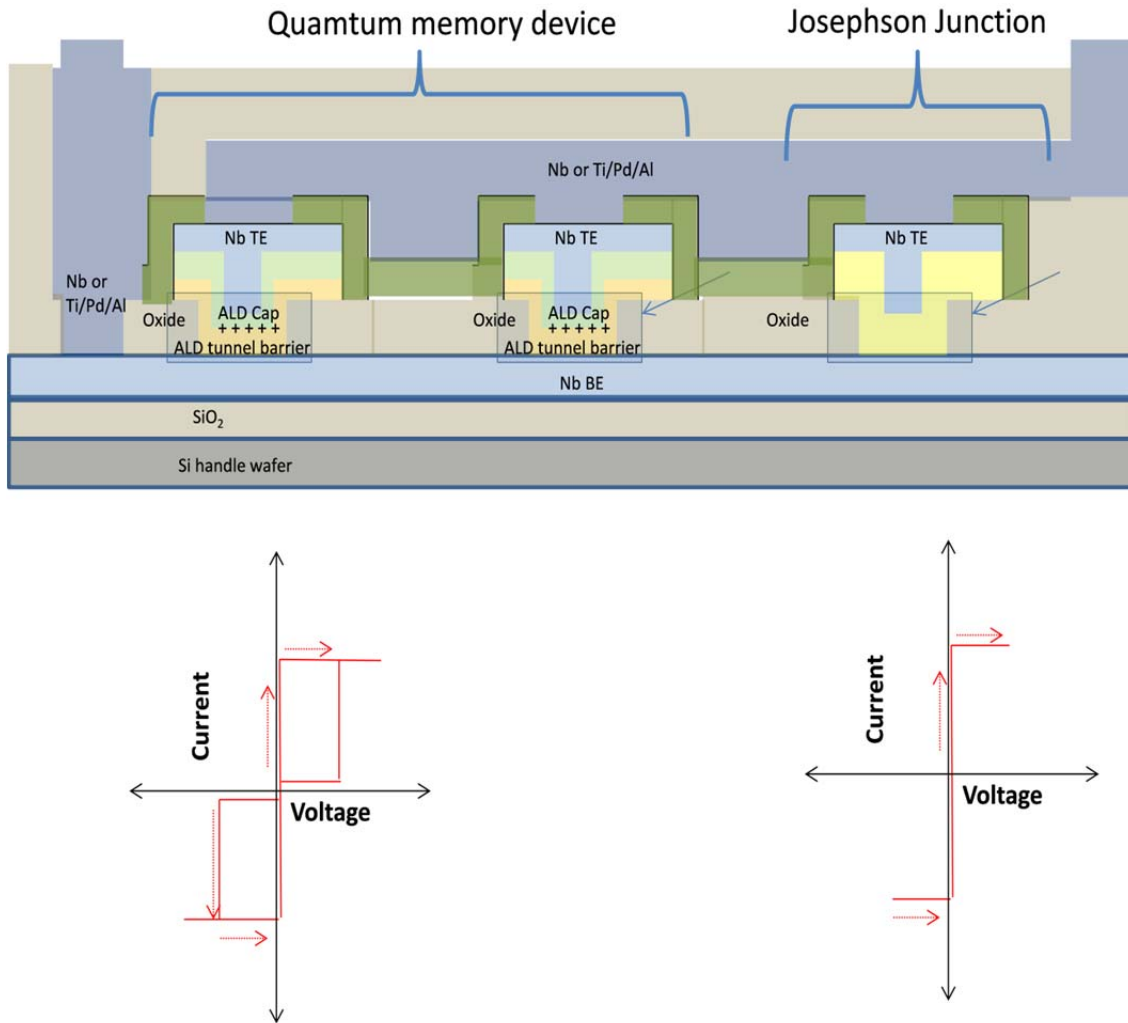


Figure 48. Heterogeneous integration of Josephson junctions and quantum memory in close proximity enabled by the process.

The project is currently on track and has completed construction of a new set of devices at the Qualcomm Institute's Nano3 nanofabrication facility at UC San Diego. The devices incorporate an atomic precision deposition process for the development of the barrier films and Nb superconductor electrodes. The implemented process addresses several challenges for high quality uniformity across wafer with an operation temperature $\sim 4\text{K}$, an increase from the critical temperature for aluminum. The process also enables extreme scaling of device dimensions while maintaining high quality. In Section 6, we discuss the initial room temperature characterization of these devices. In FY15, we will present a more detailed characterization.

Table 6. Process flow for the construction of Nb-based QuMEM devices incorporating atomic layer deposition processes.

Process Step #	Description	Tool	Process notes
1	Starting substrates (Si wafers with 300-nm thermal SiO ₂)	Vendor supplied	4-inch-diameter wafers
2	Ti/Au/Nb (Superconductor) deposition	Sputtering	Ti: RF sputter at 200 W (6 min) ~12 nm from profiler Au: DC sputter at 300 W (6 min) ~200 nm Nb: DC sputter at 300 W (6 min) ~100 nm
3	Barrier/Ionic/Barrier deposition	Atomic layer deposition	AlO _x : 20 cycles TMA+H ₂ O at ~1 angstrom per cycle HfO _x : TDMAH + H ₂ O 20 cycles at ~1 angstrom per cycle AlO _x : 20 cycles at ~1 angstrom per cycle
4	Top Nb superconductor electrode deposition	Sputtering	Nb: DC sputter at 300 W 11 min, ~250 nm
5	Photolithography (top-electrode)	Mask aligner	Positive resist Resist developer (~40 sec)
6	Reactive-ion etching (RIE)	Plasma etch	SF ₆ for ~10 min through stack stopping at Au
7	Passivation/isolation oxide deposition	Plasma deposition	Silane and N ₂ O 7 min, ~500 nm
8	Photolithography (contact)	Mask aligner	Positive resist Resist developer (~40 sec)
9	Contact etch	Plasma etch	CF ₄ /O ₂
10	Via/bond pad deposition (Ti/Au)	Sputtering	Au: DC sputter at 300 W 6 min, ~
11	Photolithography (metal)	Mask aligner	Positive resist Resist developer (~40 sec)
12	Metal etch	Wet Bench	Wet etchant

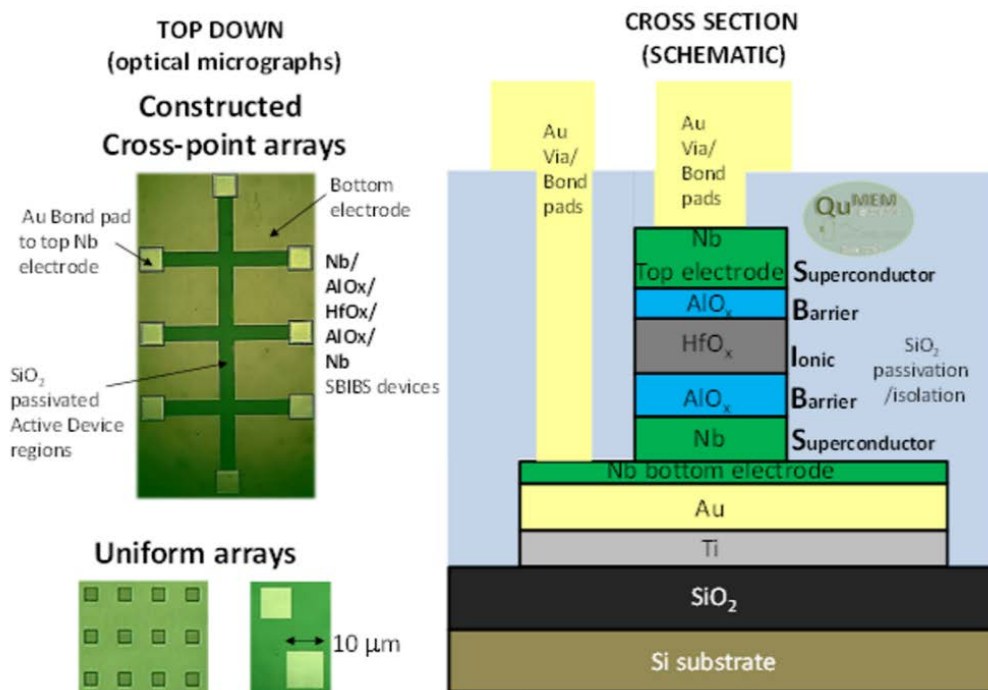


Figure 49. Optical micrographs and schematics of Nb-based QuMEM devices incorporating Nb thin films and atomic precision deposition processes. The process utilizes the delivered mask set and produces both cross-point array devices and as uniform arrays.

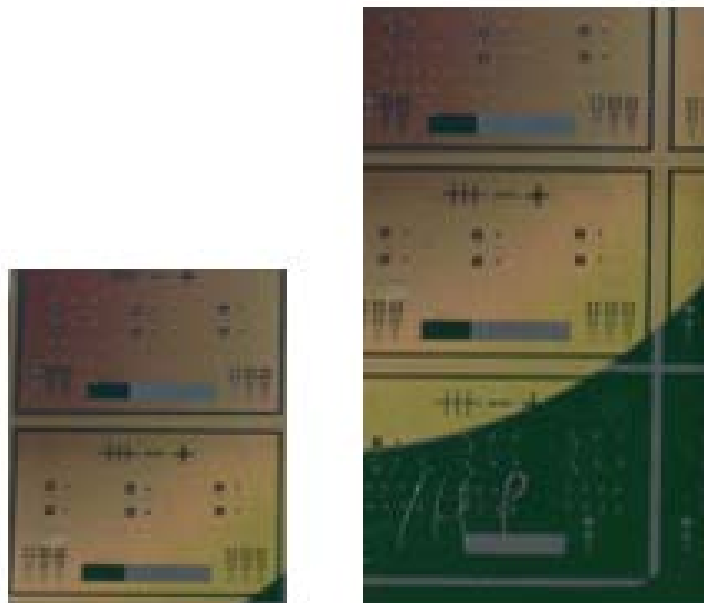


Figure 50. Constructed Nb-based QuMEM device chips on 4-inch Si wafers.

7. DEVICE CHARACTERIZATION

7.1 ELECTRICAL CHARACTERIZATION OF AL/AL_{O_x}/AL (PLASMA-MODIFIED)/AL DEVICES AT LOW VOLTAGE

We characterized constructed devices utilizing a probe-station in the SSC Pacific MEMS Laboratory connected to a Hewlett Packard® 4145 Parameter Analyzer. Measurements were performed in the moderate voltage regime <200 mV to study and understand (hysteretic) memory effects and quantum processes at room temperature. Figure 51 shows electrical measurements and simulations demonstrating resonant tunneling. Figure 52 shows electrical measurements of devices that were exposed to various plasma conditions.

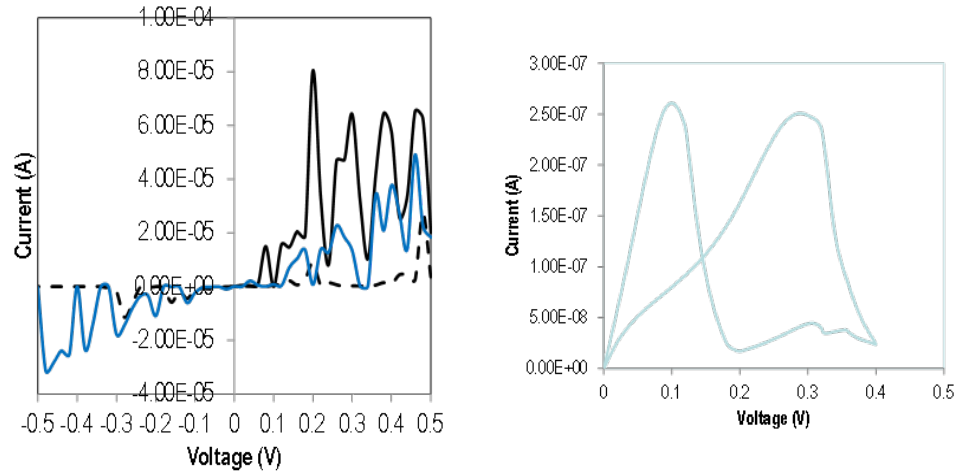


Figure 51. Electrical measurements (left) demonstrating resonant tunneling process. Good agreement is obtained between simulations (right).

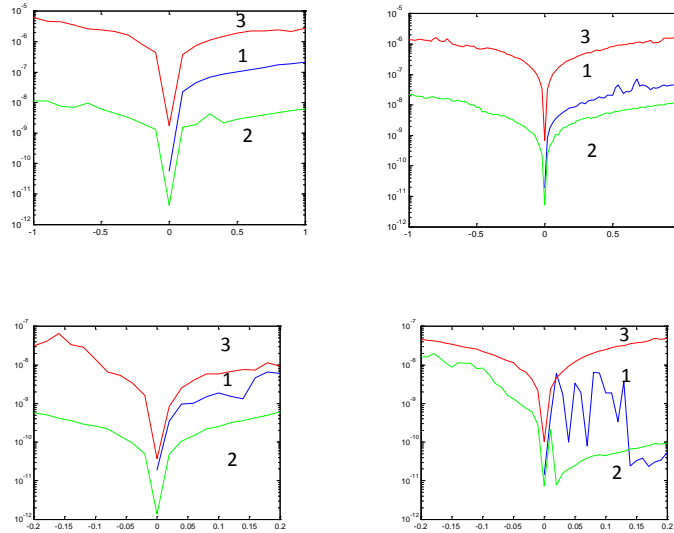


Figure 52. Electrical measurements in forward and reverse directions with increasing ionic concentration. Starting from the upper left and clockwise (5-sec oxidation, 10-sec oxidation, and CF4).

7.2 CRYOGENIC TESTING OF QUMEM DEVICES

We applied for funding for an equipment proposal for a cryogenic probe station to enable the on-chip cryogenic testing of devices. In FY14, we developed a proposal to procure a cryogenic probe station at SSC Pacific.

8. EMERGING QUANTUM DEVICES WITH ATOMIC CRYSTALS AND HETEROSTRUCTURES

Recent advances in the synthesis and isolation of two-dimensional (2-D) atomic crystals, including graphene and the broader class of transition metal dicalcogenides, are enabling the study and demonstration of devices that operate based on quantum effects and properties. So-called Van der Waals materials and heterostructures are formed with unique properties. Synthesis is either direct or cleaving and stacking. Such materials have properties favorable for devices based on quantum properties and behavior:

- High-quality material/interfaces (long coherence)
- Tunable properties and strong electric field across (\sim nm) barriers
- Quantum transport sensitive to angstrom-scale modulation
- Novel interface phenomenon/band-offsets due to atomistic ordering
- Unlimited functionality (e.g., superconductor, ionic, and [ferro] magnetic/electric)
- Simple synthesis and stacking
- High-density integration and scaling

8.1 QUMEM DEVICE DESIGN WITH 2-D CRYSTALS

Due to the ability to stack various 2-D crystals with high-quality interfaces, novel heterostructures are formed with unique and tunable properties. We are studying a design such as in Figure 53 of a Josephson device structure formed from $\text{NbSe}_2/\text{NbS}_2/\text{NbSe}_2$. At 0 V, Josephson junction tunneling of Cooper pairs can occur across the barrier of the device (e.g., NbS_2) with a critical current density J_c . Figure 54 shows a schematic of how a QuMEM device with ionic modification could be formed based on 2-D crystals.

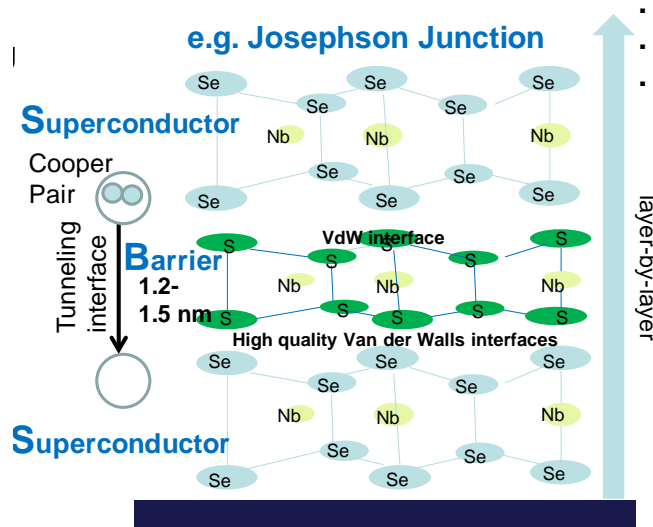


Figure 53. Josephson device constructed utilizing 2-D atomic crystals.

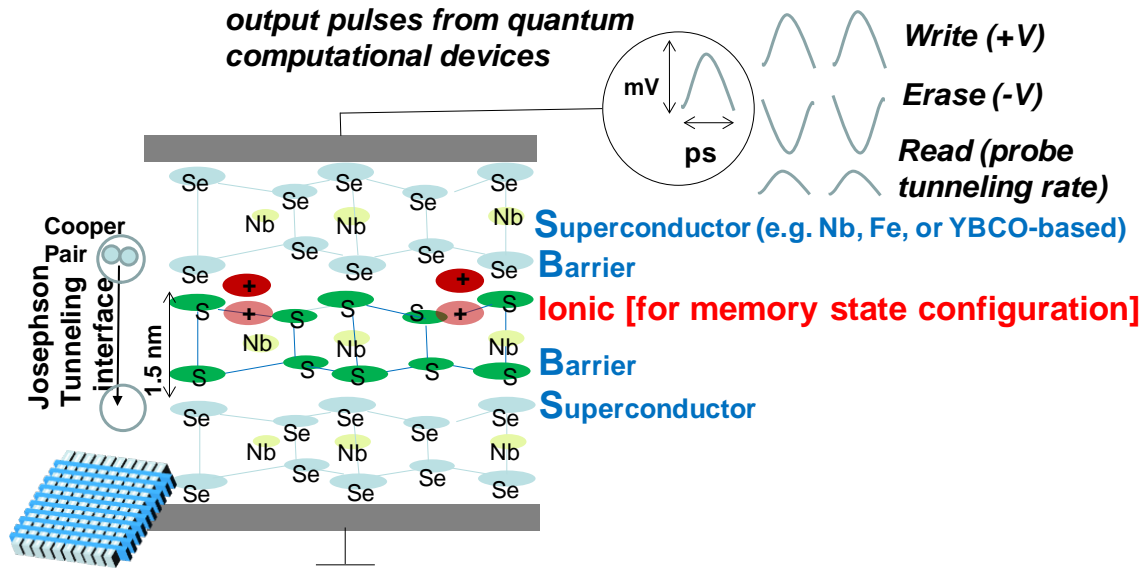


Figure 54. Schematic of device concept based on emerging high-quality 2-D crystals and interfaces (e.g., NbSe₂/NbS₂) where electric field is enhanced due to atomically thin films and heterostructure engineering and the ionic transport process is enabled at a lower voltage.

8.2 INTEGRATION OF MAGNETIC THIN FILMS FOR SPIN ORDERING

The ability to form high-quality films and interfaces also opens new possibilities for the integration of atomic crystals that have ferroelectric/magnetic properties (Figure 55). Such structures can be used for achieving the desired spin ordering.

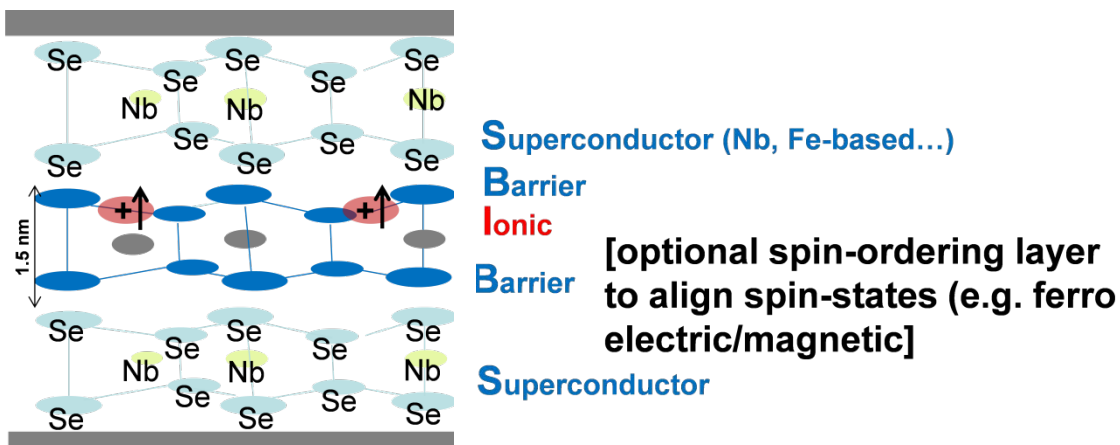


Figure 55. Due to ability to integrate arbitrary 2-D crystals, a magnetic spin-ordering film is proposed if alignment of spin states is required to maintain phased across the device.

8.3 PROGRESS OF 2-D CRYSTAL-BASED DEVICES

Figure 56 shows the in house station for cleaving and examining 2-D crystals. Figure 57 shows starting synthetic bulk crystal. Figure 58 and Figure 59 demonstrate the Scotch[®] Tape cleaving and transfer of material to SiO₂ substrates. Figure 60 shows optical micrographs, where 2-D crystals are isolated and located based on number of layers with the presence of monolayers.

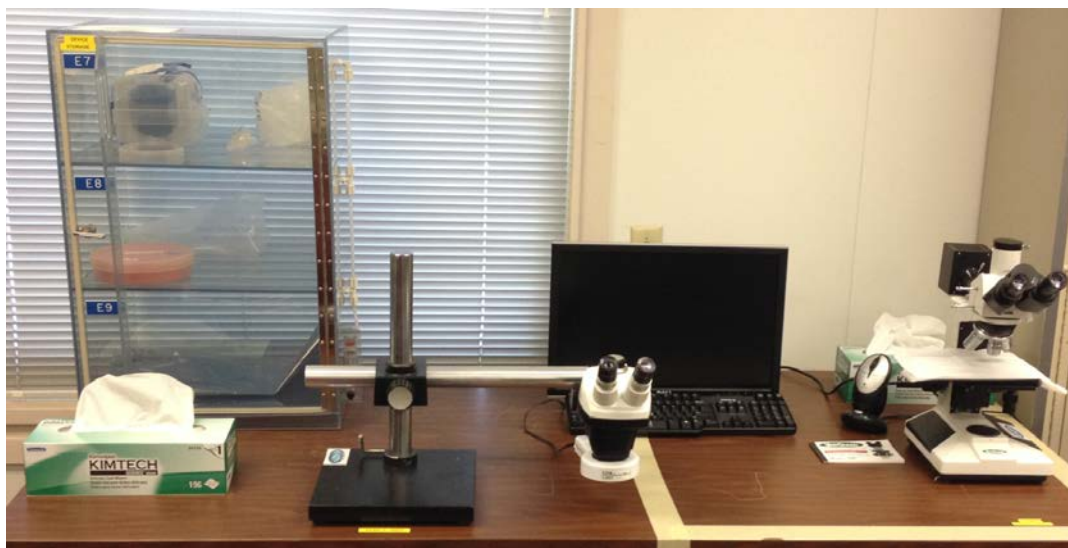


Figure 56. In-house station at SSC Pacific for cleaving and examining 2-D crystals.



Figure 57. Starting material NbSe₂ synthetic (bulk) crystal.



Figure 58. Cleaving of NbSe₂ with Scotch[®] Tape method.

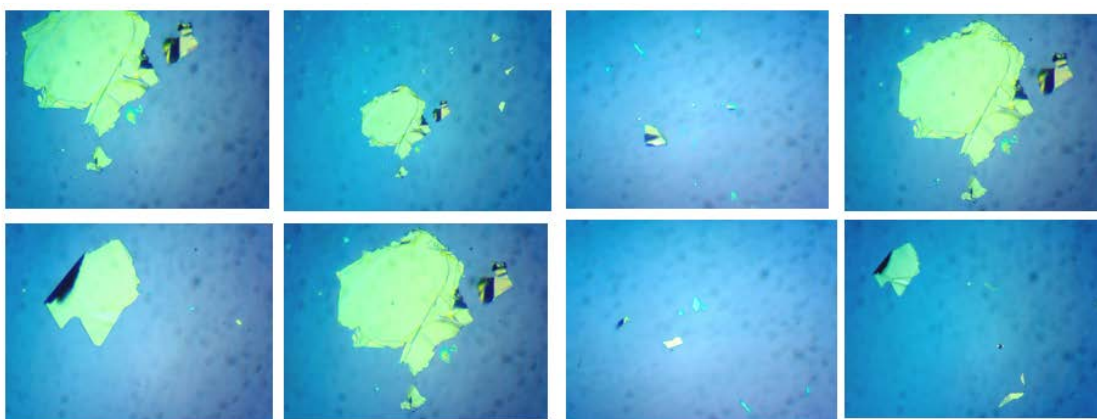


Figure 59. Transfer of NbSe₂ atomic crystals to SiO₂.

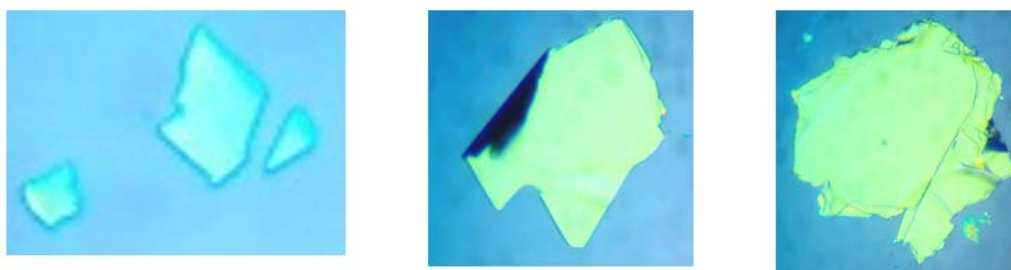


Figure 60. Locating NbSe₂ 2-D crystals with the contrast method.

9. TECHNOLOGY TRANSITION

We informed SSC Pacific program offices (PMWs) of project progress and success to enable maximum readiness for development and insertion of quantum computing technologies in their programs of record.

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14. ABSTRACT <p>This technical report presents the progress of the Space and Naval Warfare Systems Center Pacific (SSC Pacific) Nonvolatile and Cryogenic-Compatible Quantum Memory Devices (QuMEM) research project supported by the Navy's Science and Technology (S&T) In-house Laboratory Independent for Research (ILIR) Program. This report provides background information, motivation, technical progress, and technology transition efforts conducted throughout Fiscal Year (FY) 2014.</p> <p>The primary objective of the QuMEM project is to design and implement novel concepts, designs for solid-state, cryogenic-compatible quantum memory device chips where writing, reading, and erasing operations perform using fast (psec), low-voltage (mV) electrical pulses generated by on-chip computational devices. Here, quantum states are generated, tuned, and stored for computation. We increase the understanding of the memory storage process by characterizing the charging/discharging process, retention time, and endurance and how it correlates with design-driven theoretical calculations.</p>					
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